ANALYSIS OF RESTRICTED EARTH FAULT RELAY APPLICATION WITHIN A SHUNT CAPACITOR BANK DESIGN IMPACTING ON PROTECTION STABILITY

W.MINKLEY

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Analysis of Restricted Earth Fault relay application within a Shunt Capacitor Bank Design impacting on protection Stability

By:

Warick Minkley

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Supervisor: Dr. W.Phipps

Co-Supervisor: Dr. R.T.Harris

Industry -Supervisor: Mr A.M.A. Craib
In accordance with Rule G4.6.3 of the prospectus, I Warick Minkley, student number 212338749 hereby declare that the above-mentioned dissertation for the degree of Masters Technology: Engineering: Electrical is my own work and that it has not previously been submitted for assessment or completion to another University or for another post graduate qualification.

Name: Warick Minkley
Date: 30 December 2013
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This research is aimed at analyzing the performance of the restricted earth fault relay used on a 400kV capacitor bank scheme used on the Eskom Transmission network. After the commissioning of two Capacitor Banks using the above mentioned scheme design the plant was energized. As a result of the energization the Shunt Capacitor Bank (SCB) then experienced spurious trips. The cause of the trips was found to be the operation of the restricted earth fault relay.

In this research project, restricted earth fault protection on SCBs in the Eskom Transmission environment will be the area of interest. The proposed research will analyze the current SCB protection scheme in service specifically looking at the restricted earth fault circuit design and relay performance. An equivalent model of the SCB from primary plant perspective based on theory will be derived. Recording and analyzing of Comtrade transient waveforms respectively, when the bank is energized, will be done in order to provide a reference base to work from. Manual calculations of various parameters from the derived model including transient inrush currents and fault currents will be performed to access applicable scheme parameters. Further calculations will include the voltage setting for the restricted earth fault relay.

As a result of the analysis a recommendation will be made on a viable solution or a revised design will be put forward, based on the results, to improve the scheme’s performance. The protection scheme is used on the two 400kV 100MVAR capacitor banks 11 and 12 at Hydra Substation.
# TABLE OF CONTENTS

DECLARATION .................................................................................................................. I
ACKNOWLEDGEMENTS ................................................................................................. II
ABSTRACT ....................................................................................................................... III

TABLE OF CONTENTS ...................................................................................................... IV
LIST OF FIGURES ............................................................................................................ VI
LIST OF TABLES ............................................................................................................. IX
LIST OF CHARTS ............................................................................................................ IX

CHAPTER 1 – INTRODUCTION

1.1 PROBLEM STATEMENT .............................................................................................. 5
1.2 HYPOTHESIS .............................................................................................................. 5
1.3 PURPOSE ................................................................................................................... 5
1.4 SIGNIFICANCE ........................................................................................................... 5
1.5 LIMITATIONS OF THE RESEARCH ........................................................................ 6
1.6 OUTLINE OF THE STUDY ...................................................................................... 8
1.7 DEFINITION OF CONCEPTS .................................................................................. 10

CHAPTER 2 - REVIEW OF RELATED LITERATURE

2.1 Introduction ................................................................................................................ 12
2.2 Overview of the Existing 400kV 100MAR Grounded Wye Bank ............................ 12
2.3 Capacitor Bank Switching transients ...................................................................... 13
2.4 Methods to Reduce Capacitor Bank Switching transients .................................. 14
2.5 General Protection Elements for SCB .................................................................... 14
2.6 Restricted Earth Fault Protection ........................................................................... 18
2.7 Current Transformer Saturation ............................................................................. 18
2.8 Restricted Earth Fault Sensitivity .......................................................................... 19
2.9 Static Relay Topology ............................................................................................. 19
2.10 High Impedance Restricted Earth Fault Relay Testing ....................................... 20
2.11 Operation of Numerical High Impedance Protection Schemes Due to
In-Zone Surge Arrester Conduction ............................................................................. 22
2.12 Concerning the Use of a Surge Capacitor and Surge Reactor .............................. 23
2.13 Surge Protection of Relay Systems Associated with Capacitor Banks ................ 23
2.14 Control Cable Switching Interference ................................................................... 24
2.15 Relay Test Methods ............................................................................................... 24
2.16 Transient Simulation Testing ................................................................................ 25
2.17 Comtrade Fault Playback ...................................................................................... 25
2.18 Digital Fault Recording Event Analysis .................................................................. 25
2.19 A Software Simulation Platform .......................................................................... 26
2.20 Relay Filtering ....................................................................................................... 27
2.21 IEEE Std 1036-2010 Guide for Application of Shunt Power Capacitors ............. 27
2.22 Point on Wave Switching ...................................................................................... 28
2.23 Conclusion ............................................................................................................. 29

CHAPTER 3 – DESIGN

3.1 Introduction .............................................................................................................. 30
3.2 Capacitor Bank Calculations .................................................................................. 30
  3.2.1 Capacitor Bank Inrush Calculations ............................................................... 34
  3.2.2 Single Bank Energizing .................................................................................. 36
  3.2.3 Double Bank Energizing ................................................................................ 39
3.3 Setting Calculations for REF Relay ...................................................................... 42
3.4 Current Transformer Performance ........................................................................ 48
3.5 Energizing Recordings ........................................................................................... 49
  3.5.1 Scenario 1: Single Bank Inrush Site Recordings ............................................. 52
  3.5.2 Scenario 2: Double Bank Outrush Site Recordings ....................................... 56
LIST OF FIGURES

Figure 1.1: Power Factor Reduction by addition of capacitance to network .................................................. 1
Figure 1.2: Overall layout of the restricted earth fault relay, illustrating the key components to the design......2
Figure 1.3: Shows the 400kV 100MVAR Shunt Capacitor Bank at Hydra Substation situated in De Aar. One can see the individual capacitor elements, surge reactor and earthing capacitors respectively ..........3
Figure 1.4: Hydra Substation Single line diagram ......................................................................................... 4
Figure 1.5: Omicron CMC356 .................................................................................................................... 6
Figure 1.6: The project outline graphically illustrating an overview of the approach used in solving the problem at hand. ............................................................................................................. 9
Figure 1.7: Single line representation of the Shunt Capacitor Bank ............................................................. 12
Figure 1.8: Typical bus voltage and capacitor current transients during single bank capacitor energizing......13
Figure 1.9: Basic Elements of a static relay .................................................................................................. 19
Figure 1.10: Siemens 7VH600 High Impedance Relay .................................................................................. 20
Figure 1.11: Recording of surge arrestor conduction during a lightning strike on a 66kV network which caused a transformers REF protection to operate, the surge arrestor’s fall within the REF zone.............. 22
Figure 1.12: Typical steady state test voltages and currents ......................................................................... 24
Figure 1.13: Typical dynamic state test voltages and currents ...................................................................... 25
Figure 1.14: A layout of the bank is shown above showing all individual elements and interconnections ......31
Figure 1.15: Equivalent Source model required to be derived .................................................................... 34
Figure 1.16: DigSelenium Model used to derive system parameters ............................................................. 35
Figure 1.17: Inserting equivalent parameters for the shunt capacitor bank into the source impedance model to calculate single bank inrush currents ......................................................................................... 36
Figure 1.18: Source impedance model to calculate double bank inrush currents ......................................... 39
Figure 1.19: Single phase equivalent circuit simplification method for calculating equivalent phase impedance in the event of an earth fault ....................................................................................... 45
Figure 1.20: Current transformer burden comparisons for the CT’s used in the restricted earth fault circuit ................................................................................................................................................................. 48
Figure 1.21: An Omicron CMC356 Test Set connected to the secondary instrumentation circuits within the capacitor bank protection panel ....................................................................................................... 49
Figure 1.22: Red block waveform indicates a digital representation of the analogue waveform in the background .......................................................................................................................................................... 50
Figure 1.23: Enerlyser software setup showing the configurations used to record the current and voltage inputs into the unit ................................................................................................................................................ 50
Figure 1.24: Enerlyser software showing configuration of sampling frequency and trigger thresholds.......51
Figure 1.25: First scenario single bank energizing was recorded for the network configuration above ........52
Figure 1.26: Busbar voltages on 400kV busbar recorded whilst energising a single 400kV shunt capacitor bank ...................................................................................................................................................... 52
Figure 1.27: Recorded phase current whist energising 95MVAR 400kV shunt capacitor bank 11 ............... 53
Figure 1.28: Recorded voltage waveform during switching appearing across restricted earth fault relay on capacitor bank 11 ................................................................. 53
Figure 1.29: DFT Fourier plot of harmonic voltage content across relay element recorded while energizing capacitor ........................................................................................................... 54
Figure 1.30: Recorded voltage waveform during switching appearing across restricted earth fault relay on capacitor bank 12 ........................................................................................................... 54
Figure 1.31: DFT Fourier plot of harmonic voltage content across relay element recorded while energizing capacitor 12 ........................................................................................................... 55
Figure 1.32: Switching scenario for measurement of outrush current ................................................................................................................................. 55
Figure 1.33: Recorded outrush current waveform taken during switching appearing across restricted earth fault relay on capacitor bank 11 ........................................................................................................... 56
Figure 1.34: Recorded REF voltage during capacitor bank 11 outrush ................................................................................................................................. 56
Figure 1.35: DFT Fourier plot of harmonic voltage content across relay element recorded for outrush energizing condition ........................................................................................................... 57
Figure 1.36: Switching scenario for measurement of double bank inrush current ................................................................................................................................. 57
Figure 1.37: Recorded inrush current on 400kV 95MVAR capacitor bank 12 ................................................................................................................................. 57
Figure 1.38: Parameters used for network source model in simulation ................................................................................................................................. 59
Figure 1.39: Positive and zero sequence source impedances required for accurate transient current flow calculations ................................................................................................................................. 59
Figure 1.40: Breaker modeled as three single breaker poles with zero resistance ................................................................................................................................. 60
Figure 1.41: Breaker closing times are set to the same times as measure from site recordings taking delays into consideration ................................................................................................................................. 60
Figure 1.42: Independent breaker pole control achieved by logic timers controlling closing times ................................................................................................................................. 60
Figure 1.43: Input parameters for equivalent capacitance, this is applicable for both phase and earthing capacitance values ................................................................................................................................................................. 61
Figure 1.44: Current transformer data used in the model the parameters are derived from measured values recorded on site ................................................................................................................................................................. 62
Figure 1.45: ABB Plexim surge arrester Data Sheet ................................................................................................................................................................. 63
Figure 1.46: Basic parameters of the surge arrester used in the PASCAD model and specification of its I-V characteristic ................................................................................................................................................................. 63
Figure 1.47: The 30/60 microsecond wave front characteristic is used to model the surge arrester the data is used to populate the I-V characteristic table required in the model ................................................................................................................................................................. 63
Figure 1.48: Single capacitor bank energizing inrush current switching model constructed in PSCAD ................................................................................................................................................................. 64
Figure 1.49: Simulated phase current while energizing a single 400kV shunt capacitor bank in PSCAD ................................................................................................................................................................. 65
Figure 1.50: Simulated REF voltage while energizing a single 400kV shunt capacitor bank in PSCAD ................................................................................................................................................................. 65
Figure 1.51: Double capacitor bank energizing inrush current and outrush current model constructed in PSCAD ................................................................................................................................................................. 66
Figure 1.52: The switching instances for each pole are set to be the same as the original recorded waveform ................................................................................................................................................................. 66
Figure 1.53: Simulated REF voltage whist induced by outrush current whist energizing an opposite 400kV shunt capacitor of equivalent size bank on local busbars in PSCAD.................................................. 67

Figure 1.54: Simulated REF voltage whist induced by outrush current whist energizing an opposite 400kV shunt capacitor of equivalent.............................................................................................................. 67

Figure 1.55: Surge arrestor conduction during energizing of capacitor bank .................................................................................. 68

Figure 1.56: Relay operate times for an increase in voltage above the setting voltage................................................................. 70

Figure 1.57: 7VH600 tripping time speed when injected with voltages with higher magnitudes and frequencies............................................................................................................. 70

Figure 1.58: Typical RC filter topology .............................................................................................................................................. 71

Figure 1.59: Basic test principle used for testing REF relay filtering. Indicates where capacitors are added to improve filtering circuitry .............................................................................................................. 72

Figure 1.60: Standard filter response to setting voltage .................................................................................................................. 73

Figure 1.61: Modified filter response to setting voltage .................................................................................................................. 73

Figure 1.62: Injected transient recorded waveform and relay response to standard filter ................................................................. 74

Figure 1.63: Injected transient recorded waveform and relay response to modified filter .................................................................. 74

Figure 1.64: Injection of 20% 2nd harmonic superimposed on fundamental into standard filter .......................................................... 75

Figure 1.65: Injection of 20% 2nd harmonic superimposed on fundamental into modified filter .......................................................... 75

Figure 1.66: Recorded inrush current during energizing of capacitor bank 12 with capacitor bank 11 in service .............................................................................................................................................. 82

Figure 1.67: R.M.S representation of voltage across filter circuit during single bank energizing conditions .............................................................................................................................................. 84

Figure 1.68: R.M.S representation of voltage across modified filter circuit during single bank energizing condition with modified filter showing reduction in voltage .................................................................................. 85
LIST OF TABLES

Table 1-1: Parameters for a single capacitor can element found within the shunt capacitor bank ...................... 31
Table 1-2: Parameters for a single earthing capacitor can element found within the shunt capacitor bank .............. 32
Table 1-3: Parameters for a single earthing capacitor can element found within the shunt capacitor bank ............ 33
Table 1-4: Parameters sourced from Digsilent Power Factory for three and single phase bolted earth faults on the local 400kV busbars at Hydra Substation ................................................................. 35
Table 1-5: Protection circuit parameters required for setting calculations .............................................................. 42
Table 1-6: Range of settings available for selection for the restricted earth fault relay ....................................... 43
Table 1-7: The following table illustrates the reduction in phase impedance for earth fault locations at different points in a single string ........................................................................................................... 47
Table 1-8: Closing Times used for poles derived from recordings ......................................................................... 60
Table 1-9: Inrush current peaks in secondary circuit of recorded values vs simulation values ............................ 78
Table 1-10: Standard relay circuitry response when a nominal setting voltage is injected with 20% harmonic content superimposed on fundamental ........................................................................... 86
Table 1-11: Modified relay circuitry response when a nominal setting voltage is injected with 20% harmonic content superimposed on fundamental ........................................................................... 87

LIST OF CHARTS

Chart 1-1: Harmonic analysis of the 400kV busbars voltage with the capacitor is switched onto ......................... 79
Chart 1-2: Harmonic content of recorded voltage across restricted earth fault relay element for single bank in rush capacitor bank 11 ........................................................................................................... 79
Chart 1-3: Harmonic content of recorded voltage across restricted earth fault relay element for single bank in rush capacitor bank 12 ........................................................................................................... 80
Chart 1-4: Simulated harmonic content of voltage appearing across restricted earth fault relay for single bank energizing condition ....................................................................................................... 81
Chart 1-5: Harmonic analysis of percentage difference for recorded current waveforms for outrush and inrush conditions .......................................................................................................................... 82
Chart 1-6: Harmonic analysis of recorded REF voltage waveform for outrush of capacitor bank 11 energizing capacitor bank 12 ........................................................................................................... 83
Chart 1-7: Simulated voltage appearing across restricted earth fault relay during outrush ................................ 83
Chart 1-8: Percentage of harmonics in standard filter circuit when injected with energizing transient waveform .............................................................................................................................. 85
Chart 1-9: Percentage of harmonics in modified filter circuit when injected with energizing transient waveform .............................................................................................................................. 86
CHAPTER 1 - INTRODUCTION

During the winter of June 2006, two 400 kV shunt capacitor banks were installed at Eskom’s Hydra Substation near De Aar. The two capacitor banks were the first phase of an order received by Eskom’s Capital Expansion Department to design, supply and install a total of six 100 MVAR, 400 kV shunt capacitor banks at the Hydra, Perseus and Beta Substations on the 400 kV transmission system which feeds the Western Cape.

The project was one of several planned by Eskom to increase the transmission capacity of the high voltage system supplying the Western Cape. It required a rapid response with respect to commissioning in the light of the well-publicised load restrictions in the first half of 2005.

Installation of capacitor banks near load centres assist in the reduction of reactive power being drawn by the reactive network loads. When power factor angles start diminishing the installation of these capacitor banks can assist in rectifying the load angle bringing it closer to zero as well as the power factor closer to unity. Capacitor banks provide a cheap viable solution in this regard and take less time to install when compared with other solutions. The capacitor bank is of the switched type, which means it can be switched in or out of service as the power system network controller requires.

![Figure 1.1 Power Factor Reduction by addition of capacitance to network.](image)

Shunt capacitor banks assists in reducing the networks total reactive power load as well as decreasing the power factor angle as portrayed in figure 1.1. By reducing total reactive power the current drawn by the network is reduced resulting in less of a voltage drop across heavily loaded long lines.

Each phase of the shunt capacitor bank (SCB) is constructed in two stacks or banks interconnected by cables with capacitively earthed neutrals so that a conventional voltage differential protection scheme can be used. The bank is of the fuseless construction which is preferred by Eskom because this technology has proven to be reliable and easy to maintain [1]. Fuseless capacitor banks mainly utilize an unbalance protection scheme as the
primary means of protection. As the name implies, there are no internal or external fuses on this design. Their "string" configuration provides a very reliable and cost effective design for banks rated at 35 kV and above [2].

During the final commissioning phase when one of the Shunt Capacitor banks was energised the Restricted Earth Fault (REF) relay operated spuriously. Spurious operation during energization was also confirmed on the other opposing bank when it was in service during this time.

Restricted earth fault protection is designed for fast and selective differential protection. The two SCB concerned use high impedance Restricted earth fault protection which uses a circulating current principle. The zone of protection lies between current transformers which encompass the plant it is protecting. Therefore the unit being protected is the entire bank from the area before the 400kV circuit breaker to the neutral point of the SCB. A faulty element within this zone of protection could thus cause an unbalance of current and cause a restricted earth fault (REF) condition.

![Diagram](image)

Figure 1.2 Overall layout of the restricted earth fault relay, illustrating the key components to the design.

The use of a surge arrester in the zone of protection can increase the possibility of a REF operation when the bank is energized. This can be attributed to the surge arrester conducting during switching due to temporary switching overvoltage’s within the bank. The temporary overvoltage’s are caused by the inrush currents this phenomenon normally occurs just after the breaker closing instant. If the voltages exceed the surge arrester rating it will conduct current. The conduction of the surge arrester may cause an imbalance in the REF circuit, thus causing unwanted REF relay operation. The back to back energizing of shunt capacitor banks can also contribute towards this problem as they induce large amounts of inrush currents to flow through the substation.
which can result in current transformer saturation. In addition transient current causing transformer saturation can also cause imbalances in REF circuitry.

Maximum availability of these capacitor banks for service requires reliable protection which will isolate the capacitor bank from the system before it is exposed to severe damage and certainly before a fault can be established on the system. Spurious protection operations can hinder a plant’s availability and in some cases cause adverse system conditions on the network. Analyzing every unexplained relay operation (even when the cause seems apparent) builds a knowledge base and insight into the operation of the protective schemes that can pay off in the future [3].

Figure 1.3 Shows the 400kV 100MVAR Shunt Capacitor Bank at Hydra Substation situated in De Aar. One can see the individual capacitor elements, surge reactor and earthing capacitors respectively.
Figure 1.4 Shows the single line diagram representation of Hydra Substation indicating the location of Capacitor Bank 11 and Capacitor Bank 12 on the 400kV Busbars. Hydra Substation is substantially large and consists of multiple incoming and outgoing feeders and transformers as well as static var compensators.
1.1 PROBLEM STATEMENT

Two 400kV shunt capacitor banks at Hydra Substation, namely Capacitor bank 11 and 12, are tripping at the point of energization. The cause of the trip has been pinpointed to be the REF relay of the protection scheme.

1.2 HYPOTHESIS

1.2.1 Secondary transient energizing record injection of the REF relay will prove its designed operational characteristics and security during transient fault conditions. If the secondary injection of the transient Comtrade recordings which is recorded during energizing conditions proves unreliable operation of the REF relay and limited susceptibility to harmonics, the research objective will focus on the REF circuit design.

1.2.2 In the case where relay security is compromised due to unreliable operations redesigning of the REF circuit will be necessary to increase relay security. The aim is to prove that REF protection can be applied in the SCB circuit.

The Comtrade format is a collection of data around an event point, recorded at regular time intervals, to define the characteristics of voltage, current and the status of digital channels before, during, and after an event. This can be played back through digital test instruments, via a PC, to replicate the genuine event as it occurred on the system. [4]

1.3 PURPOSE

The purpose is ultimately to ensure secure and reliable operation of the capacitor bank. The aim is to diagnose the root cause of the trip and authenticate its accuracy. The investigation into the relay filtering circuitry will provide insight into identifying shortcomings in relay filter design and applications. The restricted earth fault relay circuit should remain stable during system transient conditions.

1.4 SIGNIFICANCE

It is possible to optimize the voltage profile on a network. One of the ways this can be achieved is by the installation of shunt capacitor banks. There are numerous protection philosophies which are applied to protect these capacitor banks in order to protect them from lightning strikes, switching operations and network faults. The availability of these SCB at Hydra Substation is important in terms of voltage stability to the Western Cape network. Therefore reliable operation is of utmost importance to system operations. System downtime on this plant must be limited. Thus it is imperative that unexplainable trips must be investigated and remedied.
The use of restricted earth fault protection is being more frequently used in unit protection systems. REF protection is typically applied to power transformer protection systems, and there is little documentation with regard to its use within capacitor banks. Therefore sound knowledge of its operational characteristics and behavior is key to system reliability and security.

1.5 LIMITATIONS OF THE RESEARCH

The proposed research focuses on Hydra Substation’s 400kV 100 MVAR Shunt Capacitor Bank 11 and 12 shown in Fig 1.4 in conjunction with the design of the REF circuit and high impedance REF protection relay operation. Three digital Comtrade recordings of the energizing phenomenon of the schemes in service was made. This is done using a suitable fault recorder and applicable software such as a Omicron 356. This recording will be implemented in the calculations as well as the testing of the REF relay.

A Software simulation was conducted to try replicate and verify the recordings taken on site. The calculations will consist of a transient inrush current analysis of the shunt capacitor bank and harmonic analysis of the three recorded waveforms. The testing of the relay will be performed using the Omicron 356 as seen below in figure 1.5. Analysis of probable surge arrestor conduction within the capacitor bank will not be fully examined but will be briefly discussed. In cases where system parameter values are not obtainable suitable assumptions will be made.

Figure 1.5 Omicron CMC 356

Figure 1.5: Shows an Omicron CMC356 test set used to take current and voltage recordings. Similarly the test set functions as secondary injection unit and is used to test the restricted earth fault relay. Courtesy www.omicron.at
The busbar impedances in the inrush calculations are assumed to be ideal or of zero impedance, however the series surge reactor influence is considered. The inductive value of the series surge reactor is much larger than the busbar reactance and will therefore have a greater influence on inrush currents. Similarly coupling capacitances between pieces of plant are also not considered and assumed to be zero as the capacitance of the bank far overshadows these magnitudes. The effect of neglecting these impedances will cause the calculated inrush currents to be marginally higher than in reality.

The testing of the relay will include testing the relays input filtering circuits response to the recorded transient type faults as well as its general operational characteristics when exposed to a range of harmonic voltages mainly from 50Hz extending to 250Hz. This will also include exploring the addition of additional circuitry to improve filter performance. Relay setting parameters are calculated based on inrush calculations and system parameters. This is achieved by applying network theory and calculating the settings systematically. These calculations on based on parameters derived from the system operator Digsilent software model and are dependent on its accuracy. Furthermore during a nominal busbar voltage of 1p.u is used for all applicable calculations.

The results of the hand calculations as well as Comtrade fault record injection with the CMC356 will provide insight into current design operation of the REF relay. Upon discovery of possible design error’s corrective actions will be made to current REF circuit design. Modifying the design will alter the relays operating time the maximum allowable acceptable tripping time will be one and a half cycles at the setting voltage.
1.6 OUTLINE OF THE STUDY

The research has provisionally been planned to include the following chapters. Introduction and review of applicable literature. The collection followed on by interpretation and analysis of data. The testing of the relay circuitry and characteristics, and finally by conclusion and recommendations.

- **Chapter One** sets out the background and aims of the research. It deals with the research question, assumptions, the research objective and importance of the study. Lastly the limitations of the study are highlighted.

- **Chapter Two** is a review of the relevant literature required to investigate and formulate a suitable approach to solve the problem. The review starts with basic concepts regarding shunt capacitor bank protection and progresses to scenario and application specific situations. The review’s goal was to achieve clarification and guidance of the situation at hand.

- **Chapter Three** covers the research strategy and methodology. This involves inrush fault studies and setting calculations for the restricted earth fault relay and includes system simulations. Recording and capturing fault records for switching events. Testing the restricted earth fault relay and filter’s performance.

- **Chapter Four** results are reported, analysed and discussed.

- **Chapter Five** provides the summary of the research findings, conclusions and recommendations.
Figure 1.6: The project outline graphically illustrating an overview of the approach used in solving the problem at hand.
1.7 DEFINITION OF CONCEPTS

- **Capacitor Bank**: Is an assembly at one location of capacitor units and all necessary accessories, such as switching equipment, protective equipment, control, etc. that is required for a complete operating installation. It may be a collection of components assembled at the operating site or may include one or more piece(s) of factory assembled equipment.

- **Capacitor Element**: A device, which captures an electrical charge when placed in the presence of an electrical field. This device consists of wound sheets of polypropylene film insulation material wrapped in aluminium foil conductors. The ability to keep this charge is measured in Farads \([F]\). This device consists of two conductive plates, which are separated by a dielectric material. The capacitance is a function of the area of the plates, the distance to which the plates are placed apart from each other and the permeability of the dielectric material used.

- **Capacitor Inrush Current**: The transient charging current that flows in a capacitor when a capacitor bank is initially connected to a voltage source.

- **Capacitor Outrush Current**: The high-frequency, high-magnitude current discharge of one or more capacitors into a short circuit. An example is the discharge into a failed capacitor unit connected in parallel with the discharging units, or into a breaker closing into a fault.

- **Capacitor Unit**: Is an assembly of capacitor elements, which are pressed together and connected in parallel and series combinations and packed into a steel container (case), with terminals brought out which are intended to introduce capacitance into an electric power circuit.

- **Comtrade**: A new IEEE standard developed by the IEEE PES Power System Relaying Committee. It is intended for use by digital-computer-based devices which generate or collect transient data from electric power systems. The standard facilitates an exchange of the transient data for the purpose of simulation, testing, validation, or archival storage.

- **Externally Fused Capacitor Unit**: A capacitor unit having fuses mounted on its terminals, inside a terminal enclosure, or inside the capacitor case, for the purpose of interrupting a failed capacitor.

- **Filter Bank**: A filter bank is a combination of a high voltage shunt capacitor bank and a reactor (usually connected in series) chosen such that they form a resonant circuit for a specific frequency that needs to be filtered out of the power system grid. The resonant circuit is usually tuned for a specific frequency (harmonic) and forms a low impedance path for the harmonic energy to flow to earth.

- **Fuseless Capacitor Unit**: Is a capacitor unit without any fuses, internal or external, which is constructed of parallel strings of series-connected capacitor units between line and neutral (wye connection) or between line terminals (delta or single-phase).
- **Harmonics**: Harmonics are specific frequencies that are multiples of the fundamental frequency.

- **Internal Fused Capacitor Unit**: A capacitor unit with fuses inside, which are connected in series with an element or a group of elements.

- **Power System**: Is a network that includes the point where power is generated together with the transmission networks and ending at a distribution level. A system of high tension cables by which electrical power is transmitted through the system.
2.1 **INTRODUCTION**

The design of SCB has steadily evolved over time as new technologies have become available to the engineer. Fortunately the fundamentals of their design remain the same. A review of various high voltage SCBs will reveal what topologies are in use in the Eskom Transmission system and will provide information into the layouts of the protection schemes. One of the key tools for the research will be Comtrade fault playback and recordings. An appropriate recorder and associated software package will need to be decided on to conduct the recordings and fault playback. The tolerances for the test set will also need to be noted.

The plausible application of high impedance REF protection needs to be explored. The specifications of the REF relay need to be obtained from manufacturers data sheets to verify its filtering techniques and response to harmonics. Methods used for harmonic transient and fault magnitude calculations need to be studied in order to perform the relevant manual calculations. All the required information will be gathered by reading related books, recently published journals, internet and other research pertaining to these fields.

2.2 **OVERVIEW OF THE EXISTING 400KV 100MVAR GROUNDED WYE BANK**

Figure 1.7 illustrates the single star earthed bank in a single line diagram form. The capacitor bank itself indicates the star connection on a per phase basis. The outdoor bay comprises of the following switching devices; busbar isolators (off load switching), a circuit breaker for on-load switching and for the isolation of faults, earth switches for safety and maintenance purposes.

The purpose of the reactor is to detune the dominant harmonic current. This includes presenting the shunt compensation as an inductive quantity to the network in order to mitigate resonance between the capacitor bank and the inductive overhead line. Instead the series reactor resonates with the capacitor with the affect that their resonant magnitudes cancel each other out.

![Figure 1.7 Single line representation of the Shunt Capacitor Bank.](image)
2.3 CAPACITOR BANK SWITCHING TRANSIENTS

Capacitor bank switching transients is not a new phenomenon. When a capacitor is connected to a power source it initially appears as a short circuit. This is because the voltage across the capacitor cannot change instantly. It requires a certain amount of time to charge. The initial energizing of the capacitor will cause the voltage at the connect source to drop severely. The extent of the voltage dip and the transient step change are a function of the impedance behind the source and non-linear characteristics of the connected plant. The voltage will then improve through a high frequency oscillation. These switching transients can originate from various conditions. Listed below are some of the scenarios:

- shunt-capacitor switching, which can include switching on to a fault.
- potential secondary resonance when the capacitors are applied at different voltage levels in a system.
- tripping or de-energizing a bank under normal operation and under fault situations.
- restrikes and prestrikes in the switching apparatus.
- back-to-back switching of a second capacitor bank on the same bus in the presence of an already energized bank.

![Figure 1.8 Typical bus voltage and capacitor current transients during single bank capacitor energizing.](image)

The transient inrush current experienced when energizing a capacitor at the peak on a voltage sine wave can be seen in figure 1.8. When a capacitor is connected to a power source it appears as a sudden short circuit, this causes a brief short circuit condition. Furthermore the voltage across the capacitor cannot change instantaneously during this condition and a brief voltage dip will occur. [5]
2.4 METHODS TO REDUCE CAPACITOR BANK SWITCHING TRANSIENTS

It is common practice to limit capacitor bank switching transients by implementing the following strategies.

- Series inrush current limiting reactors
- Resistance switching on breakers
- Point on wave switching controllers
- Surge arrestors
- Dividing banks into smaller sizes therefore limiting the effects of switching one large bank.
- Avoid having capacitor banks on different voltage levels within the same substation, this could lead to secondary resonant conditions.
- Consideration of steady state voltage rise do to capacitors being switched into the network. Transformer tap positions may need to be catered for in this case. [5]

2.5 GENERAL PROTECTION ELEMENTS FOR SCB

A shunt capacitor bank is a complex array of electrical components, which when exposed to adverse forces be it electrical or mechanical outside of acceptable tolerance levels can fail. The function of the protection elements within a protection scheme is to selectively detect the onset of these abnormal electrical system conditions and remove the shunt capacitor bank from the system with speed by tripping the breaker before catastrophic failure can occur. A typical protection scheme will consist of multiple protection functions this allows the protection engineer to provide adequate protection against a wide variety of faults. Furthermore for the sake of redundancy and security these protection functions often overlap and provide a back-up protection facility for alternate elements.

Shunt Capacitor and Filter Bank Protection Functionalities

The major focus areas for capacitor bank protection include the minimizing damage due to system faults and nuisance bank operations. The introduction of modern design principals and technology has played a major role in the advancement of capacitor bank protection.

Shunt Capacitor Bank Protection

This protection should operate for faults present in the capacitor bank. The faulted capacitor element or entire bank should be removed from the system to prevent further damage in the event of a protection trip. Unbalance protection operates for an unbalance event between two banks, this will cause unbalance current to flow between the two circuits and can be used to identify capacitor element failure.
System Protection

System protection should concentrate on stresses caused by various power system conditions. These conditions include capacitor bank switching or normal network switching operations which could cause voltage fluctuations on the system. These conditions could either generate alarms or remove the bank from the system. Modern approaches may utilize differential voltage unbalance and neutral voltage unbalance protection.

“Shunt capacitor bank protection system should guard against the following faults or abnormalities:

- Continuous over voltage in excess of 110% of rated r.m.s capacitor voltage whether this is caused by capacitor unit failures or sustained system over voltages.

- Overcurrent caused by individual capacitor unit failures or capacitor bus faults.

- Arc-over within the capacitor rack.

- Discharge currents from parallel capacitor units.

- Inrush currents caused by capacitor switching.

The use of conventional overcurrent and over voltage principles, as well as unbalance and differential relaying principles, can solve many of these problems” [3]

Protection against energisation transients: Inrush Currents

The magnitude of the system voltage, surge impedance, residual charge and instant in the voltage wave when the breaker is closed will affect the magnitude and frequency of inrush currents generated during capacitor bank switching. When back to back energizing of two or more capacitor banks occur high frequency inrush currents can be generated due to the small surge impedance of the circuit. This can generate large electromechanical forces across the circuit breaker contacts which may exceed safe operational limits.

Effects of inrush currents are:

- Undesirable resonance within the system or part of the system

- Induction of voltage surges into the station control and protective cables (Earthed banks are more affected)

- Stress and damage to the CT’s used for unbalance protection (earthed banks are more affected)

The reduction of the inrush current peaks can be achieved by increasing the surge impedance of the closing circuit. The surge impedance is normally increased by adding reactors of fixed value in series with the capacitor bank phases. The reactors are designed in such a manner as to provide a high impedance at frequencies higher than the nominal power system frequency. [3]
Other system elements can be included in the capacitor bank circuit to increase the surge impedance. These include resistors and surge capacitors.

**Overcurrent Protection**

The overcurrent protection used in the protection scheme has an inverse definite minimum time and definite time characteristic. The first characteristic operates on a curve based on current magnitude the higher the magnitude the faster the relay operation time. This is used to for thermal current protection or to back up the unbalance. The second characteristic operates for a certain pre-determined magnitude of current as is referred to as the high set o/c setting. This element should not harmonics less than 25% of system frequency. The definitive time element should provide protection from faults on the incoming busbar, first 50% of the capacitor bank construction, HV damping/filter reactor and resistor. If current exceeds this setting the relay will operate instantaneously. It must not operate during bank energization.

Time delayed overcurrent protection can offer protection for the following faults inside the capacitor bank:

- Flashover between phases
- Flashover to the neutral point
- Flashover to earth

This protection should be stable during switching inrush, or outrush into an external fault or adjacent capacitor bank being switched in. [3]

**Overload Protection**

This protection is used to protect the capacitor against overload conditions. It normally uses a thermal model to simulate the temperature of a capacitor.

**Overvoltage Protection**

Overvoltage protection should protect the capacitor bank against high voltage condition’s which could damage the capacitor bank. The high voltage limit is 110% and if the bank is subjected to these high voltage it could sustain damage.

There are normally two stages of overvoltage definite time delayed protection:

- A low set overvoltage with approximately a 2s time delay.
- A high set overvoltage with approximately 0.1s time delay.
- Inverse definite minimum time (IDMT) overvoltage trip function.
Furthermore capacitor overvoltage protection should be coordinated with the overvoltage protection of the line. [3]

**Earth-Fault Protection**

The Earth fault protection used in the protection scheme has an inverse definite minimum time and definite time characteristic. The first characteristic operates on a curve based on current magnitude the higher the magnitude the faster the relay operation time. This is used to determined earth faults close to the neutral point of the capacitor bank. The second characteristic operates for a certain pre-determined magnitude of current as is referred to as the high set e/f setting. If current exceeds this setting the relay will operate.

**Restricted Earth Fault Protection**

The restricted earth fault protection relies on a current balance principle for stability. It is connected between the neutral CT and post CT’s on each phase of the bay. It will operate when the balance in the system is interrupted. The REF protection offers a great degree of stability for out of zone faults and reliable sensitivity for in zone faults.

The advantages of the restricted earth fault protection are as follows:

- Highly sensitive for in-zone earth faults.
- Offers a high level of security and stability for out-zone faults.
- The restricted earth fault relay operates on zero sequence differential current. [3]

**Breaker-Fail Protection**

The breaker fail protection relay measures current and monitors the state of the circuit breaker. If the circuit breaker auxiliary contact indicates the breaker is in the open state and the relay still measures current it will issue a breaker fail condition. This is because the breaker has opened and there is still current flow through the breaker contacts. Therefore all breakers supplying this current must be opened under a breaker fail condition.

**Unbalance Protection**

This is normally used as the main protection for faults on the capacitor bank. This protection should operate speedily to minimize the amount of damage to the bank in the event of a fault condition. The protection normally identifies changes in the capacitor bank’s properties.

**Voltage Unbalance Protection (Single Star Earthed Configurations)**

This is one of the main types of protection used in capacitor banks. It is used for internal capacitor unit failure identification. It has a relatively high sensitivity to identify small unbalances in the capacitor bank. There are normally two stages mainly the alarm and trip stage. When the neutral unbalance principle is used there is normally a compensation circuit used to balance the capacitor bank.
Circuit Breaker Pole Discrepancy

Circuit breaker pole discrepancy is a method used mainly on single pole breakers. It monitors the state of all three poles. If any one or two of the poles changes state it starts a timer and if the timer reaches it’s set time it initiates a trip to all three poles, and breaker fail condition.

Loss of HV Supply Protection

This protection should operate if there is a loss of busbar voltage. After a predetermined time the capacitor bank breaker should trip disconnecting the capacitor bank form the system. [3]

2.6 RESTRICTED EARTH FAULT PROTECTION

Restricted earth fault protection is unit protection used to detect earth faults within a area or zone encompassed by current transformers. It is mainly used on transformers for sensitive earth fault detection within the transformers windings. Similarly it is best suited to applications where the neutral is solidly earthed since fault current then remains at a high value even to the last turn of the winding, practically allowing complete cover for earth faults within the winding. It normally uses a neutral CT on one end of the winding and three CT’s connected in a wye configuration on the line side of the winding. There is little documentation regarding its application within capacitor banks. It is primarily based on the application of Kirchhoff’s current law summatting the various currents in the circuit. Under normal or healthy conditions the resultant current should ideally be zero, but due to inaccuracies and tolerances in design there is always a negligible spill current into the relay. Under fault conditions the sum of the currents will not be zero due to polarity reversals and magnitude increases and will force a resultant current through the relay causing it to operate. Due to its fast response time based on zero sequence currents it can sometimes be prone to maloperation. When applied in power transformer applications REF relays have been known to trip spuriously during switched inrush conditions. Similarly REF operation has occurred during through fault conditions where current transformer saturation has occurred due mismatched CT magnetization curves causing resultant spill current to flow. [6]

2.7 CURRENT TRANSFORMER SATURATION

Current transformer saturation is of particular interest under energizing and fault conditions on various apparatus. As the values of current experienced in these circumstances is normally large and contains various magnitudes of AC and DC components. CT saturation is normally attributed to the high DC component of the current waveforms. Therefore it is essential that CT selection process takes these scenarios into consideration. CT saturation is a concern because the secondary current of the CT is no longer a faithful representation of the primary current. This can jeopardize the security and stability of a REF protection scheme. [7]
2.8 RESTRICTED EARTH FAULT SENSITIVITY

There are two types of options available high impedance and low impedance restricted earth fault protection. High impedance REF protection is the more classical choice as it was the only initial option, but with the onset of modern numerical relays low impedance REF is now available. Each has its own disadvantages and benefits with respect to fault sensitivity. The main benefit of low impedance REF protection is that one can use CT’s with different current ratio’s and specifications negating the need for interposing CT’s. On the other hand high impedance REF protection has proven to be quite impervious to CT saturation caused by large out of zone faults. Furthermore it provides fast operating times. When using high impedance REF the engineer must insure that good quality CT’s are used in the design. The setting engineer must also decide on the appropriate coverage of the device being protected for faults close to the neutral. Faults that occur close to the neutral of the circuit cause the least amount of fault current to flow, therefore setting the relay to operate for these exact conditions may prove to be too sensitive and may cause spurious tripping. Furthermore a general belief among many engineers that the fault current generated for faults close to the neutral point of a star-connected transformer is very small and insignificant to operate the REF protection relay. This can only be said for resistance-earthed star-connected transformers. [8]

2.9 STATIC RELAY TOPOLOGY

A protective relay is essentially a device that converts an analogue signal to binary signal. The high impedance earth fault relay is a static type relay. Static protection relays usually consist of various elements being signal converters, measuring modules and output elements shown in figure 1.9. This implies the relay predominantly consists of solid state components such as transistors, diodes, resistors, capacitors and inductors. Static relays are the next step forward from electromechanical relays. They proved to be smaller and lighter, consume less power and presented a much lower burden as compared to electromechanical equivalents. Conversely they are susceptible to fluctuations in ambient temperature, voltage spikes and electrical discharge and interference. A basic outline of the High Impedance REF relay is shown below. The area of concern is the input element which includes the filter.

![Figure 1.9 Basic Elements of a static relay.](image-url)
2.10 HIGH IMPEDANCE RESTRICTED EARTH FAULT RELAY
APPLICATION

High impedance REF protection is used on the SCB which uses a circulating current operating principle. Its zone of protection lies between the current transformers which encompass the plant which it is protecting. In this particular case it includes the capacitor bank along with the current limiting reactor and earthing capacitors as well as the surge arrestors. The high impedance REF relay used in this application is a Siemens 7VH600 it is assumed that its burden is purely resistive as in the case of modern static or numerical protection. This was confirmed in the relay manual and is 1200Ω with a operating current of 20mA at a respective settable voltage. This operate current is irrespective of the voltage setting, but would exclude current drawn by the varistor installed in parallel with the element. The varistor is used to limit the voltage appearing across the relay and CT terminals under abnormal high current transient conditions.

The 7VH600 relay is a single pole sensitive current monitoring relay. The a.c. input impedance of the relay is adjusted by means of resistors connected in series. The resulting relay setting is a voltage pick-up value that is set by removing short-circuit links from the rear terminals. When a short-circuit link is screwed between the terminals, the resistor is shorted out and when the short-circuit link is removed, the resistor is in circuit. Each resistor corresponds to a voltage value which is the pickup current of 20 mA multiplied with the resistors ohmic value. The voltage setting on the relay is determined by adding up the voltage drops across the resistors which are not shorted out by short-circuit links (series resistors in circuit) plus a minimum base voltage setting. A maximum setting of 60 V (short-circuit links of the left side) or 240 V (short circuit links on the right side) is possible. On delivery, the short-circuit links are not installed.

Figure 1.10 Siemens 7VH600 High Impedance Relay
Input from the CTs is connected to terminals 1 and 2. The sensitive relay input transformer galvanically isolates the static measurement circuit of the relay from the main current transformers. The AC measured current is band pass filtered and half wave rectified into a dc voltage proportional to the input signal. This voltage is monitored by a Schmitt trigger circuit. If it exceeds the d.c. voltage that is equivalent to the relay nominal operating current of 20 mA, the trigger operates to energize the command output relay as well as the operation indicator.

Auxiliary supply is connected to terminals 30 and 31. An auxiliary supply monitoring circuit consisting of a green LED and a normally closed relay contact is provided to indicate the status of the supply, the relatively simple electronic design of the 7VH600 provides a robust and reliable relay suitable for all high impedance circulating current protection applications. [9]
2.11 OPERATION OF NUMERICAL HIGH IMPEDANCE PROTECTION SCHEMES DUE TO IN-ZONE SURGE ARRESTER CONDUCTION

Use of surge arrestors and their subsequent conduction in the zone of REF protection has been known to cause spurious REF trips. This problem is more prevalent in numerical protection relays. In the past the operation time of armature attracted type relays had inherent delays. With the modern onset of numerical type relays these delays have been dramatically reduced. The sensitivity of these relays have greatly improved. This could sometimes pose a problem as the relay could prove to be overly sensitive. Surge arrestors can provide the following benefits when installed on capacitor banks. Preventing capacitor failures upon the onset of a breaker restrike and aiding in averting repeated breaker restrikes. In limiting exposure to overvoltage’s a capacitor elements lifespan is increased whilst also assisting with resonance condition ultimately causing element failures. Furthermore limiting the propagation of transients generated from switching transients.

Figure 1.11 Recording of surge arrestor conduction during a lightning strike on a 66kV network which caused a transformers REF protection to operate, the surge arrestor’s fall within the REF zone.

This recording figure 1.11 is of particular interest as it can be used to provide a rough thumbprint in interpreting recorded waveforms for surge arrestor conduction. It can be seen that surge arrestor conduction during switching normally manifests itself as short fast spikes of reasonable magnitude. This intermediate frequency oscillatory transients of modest magnitudes may contain substantial energy, so the effects can be felt quite far electrically from the point of origin. However, during a lightning strike injection, of large amounts of energy into the power system occurs in a very short time. This causes deviations in voltages and currents which persist until the excess energy is absorbed by dissipative elements. [10]
2.12 CONCERNING THE USE OF SURGE CAPACITOR AND SURGE REACTOR

Surge capacitors are used to protect network elements against surges. They try to limit the extent of the overvoltage condition by providing a temporary energy storage facility, when the surge voltage appears across the capacitor it charges, and can reduce the steepness of the wave front of the surge. These surge capacitors are found connected between the neutral point and surge reactor of this particular shunt capacitor bank. The reactor connected in series with the equipment also serves an equal purpose. When the surge reaches the reactor, it initially appears only across the reactor, the reactor offers high impedance to the high frequency currents. The surge energy is initially absorbed in the magnetic field of current in the reactor. Its ability to store energy is limited but it can take care of low energy surges. Furthermore the surge or earthing capacitors provide a small impedance at the fundamental frequency which is used to elevate the star point potential of the bank from earth. This is required from a protection perspective as it will allow the effective use of current unbalance or voltage differential protection. [11]

2.13 SURGE PROTECTION OF RELAY SYSTEMS ASSOCIATED WITH CAPACITOR BANKS

Capacitor bank switching causes high frequency transients in the megahertz range and high energy transients in the kilohertz range which are also found when switching other high voltage apparatus. The protection relay used for the capacitor bank protection should include surge protection that is effective against both types of transients. Interference from high voltage switching operations has proven that common mode interference is normally greater than transverse mode interference. Common-mode noise is present on both the active and neutral wires and is measured with respect to ground. Noise which can be measured between the live and neutral wire is called normal-mode and is sometimes referred to as differential-mode or transverse-mode noise. With common-mode noise having the greater influence surge protection methods have mainly concentrated on limiting this noise type. The following methods can be used to reduce noise these include the correct routing of control cables, cable shielding and grounding as well as isolation. During switching transient overvoltage’s can occur in this case surge assertors can be used to limit the magnitude of overvoltage’s experienced. The switching of capacitor banks can also impose extra stresses on surge arrestors due to breaker restrike. The design engineer should take cognisance of this fact and appreciate that surge arrestors with a higher energy dissipation may be required. [12]
2.14 CONTROL CABLE SWITCHING INTERFERENCE

Due to the nature of high voltage environments, and the unique design of substations mainly consisting of high voltage primary and low voltage secondary apparatus. It is highly probable that electromagnetic induction can occur in cables running from circuits outside in the high voltage yard to within the relay control building. Although this does exist these effects are not analysed in the study. However, by improving the filtering circuitry on the protection relay unwanted non fundamental transient induced voltages can be suppressed. Switching operations in primary circuits are often responsible for damage to electric plant. In the majority of cases large currents flow over the substation earth mat, causing induced voltages in control cables. The problem with these transients is that they adversely affect digital and in some cases static devices in control and measurements systems. Older type electromechanical elements were very well insulated and required sustained signals to operate. This is in contrast to microprocessors based equipment, which is are more susceptible to overvoltage’s and overcurrent’s in control cables. [13]

2.15 RELAY TEST METHODS

Testing methods used on static relays differ from those of older type electromechanical type relays. This is mainly attributed to the low burden which static relays pose as compared to electromechanical relays. This needs to be considered when relay testing is taking place. This is attributed to the characteristics of the electronic components found within the relay and their susceptibility to failure from electrostatic discharge, insulation testing may also prove to be challenging.

2.15.1 Steady State testing

A steady state test is used to determine the setting point of the relay for a measured parameter. Phasor voltage and/or current test quantities are held stable for a duration much longer than the normal operate time of the relay such as seen in figure 1.12, and are varied in increments much smaller than the resolution of the relay. In the case of the REF relay the voltage is the operating quantity and is varied to perform the test.

![Figure 1.12 Typical steady state test voltages and currents showing state changes in current.](image-url)
2.15.2 Power system simulation test

Relays are required to respond to the transient conditions of distributed power system. By simulating the signals seen by the relay under such conditions setting the response time may be determined. Furthermore the disturbance may be simulated using the following test methods.

a) Dynamic-State Test

A dynamic state test is one in which phasor test quantities representing multiple power system conditions are synchronously switched between states. The term synchronously switched means that changes in phasor value from pre boundary values to post boundary values occur in all phasors at the same time with no discernable skew seen in figure 1.13. Power system characteristics such as high frequency and dc decrement are not represented in this test.

![Figure 1.13 Typical dynamic state test voltages and currents.](image)

b) Transient simulation test

A transient simulation test signal represents in frequency, magnitude and duration actual relay input signals received during power system disturbances. [14]

2.16 TRANSIENT SIMULATION TESTING

Transient testing provides the accurate simulation of power system events. It is an important tool the user has, to perform a thorough evaluation of protection scheme operation. Transient testing can be performed using the data created by an EMTP program or data recorded by a digital fault recorders (DFR). DFR records are generally not used for calibration testing, they are normally used for troubleshooting after a questionable operation or non-operation. Comtrade data files can assist the user to perform transient testing. Modern DFRs and digital protection equipment can record power system events in the Comtrade data file format. It is also possible to create Comtrade data files from simulation programs such as PSCAD. [4]
2.17 COMTRADE FAULT PLAYBACK

Fault recorders when used correctly provide useful information to protection engineers. They can record specific currents and voltages defined by the user under normal or abnormal system conditions. These recorded values are stored in a universal format called a Comtrade file. This file can be extracted from the fault recorder and analysed. The engineer can then study the recording and examine if the system responded correctly for the recorded condition. An example of this could be a protection operation on a bay. The recorder triggers when the breaker opens and a pre-fault and post-fault recording is made of a specified time. If the protection operated incorrectly due to an incorrect setting the fault can be saved from the recorder in Comtrade format and used to retest the relay operation. The fault recording is essentially played back into the protection relay and its behaviour observed. This type of testing provides more insight into the dynamic behaviour of the protection relay, which is often overlooked when performing static testing. [15]

2.18 DIGITAL FAULT RECORDING EVENT ANALYSIS

As digital recordings are standardised on modern protection relays the interpretation of their recorded data becomes important when analysing relay operations. In the case where no relay recording facilities are available the protection engineer can opt for a standalone digital fault recorder. The data which is recorded during the event is critical in diagnosing relay operation. Analysing recordings is not an easy process and requires in-depth knowledge of power system equipment and operation. Proper interpretation is key for the reliability and constant operation of the power system. [16]

2.19 A SOFTWARE SIMULATION PLATFORM

It is imperative that an adept software simulation package is chosen to analyse and simulate various power system conditions. The software must be capable of producing clear and accurate results when compared to real world situations. If these results can be reproduced the validation of the calculated and measured results becomes easier. There are various simulation packages on the market available for performing system studies. The integrity of the simulation results is highly dependent on the quality of the input data used to populate the model parameters. For the transient switching analysis PSCAD was chosen. [17]

Eskom currently has a model of the whole electrical network constructed in Digsilent Power Factory. The software is capable of performing transient studies and calculations. However in this research Digsilent was only used for typical fault analysis to derive network impedances. [18]
2.20 RELAY FILTERING

The majority of system fault calculations are derived by using the base power system frequency. Protection relays are normally required to operate if set thresholds are triggered in their setting parameters. These setting thresholds are normally derived by classical network fault calculations. Therefore the protection relay must be able to measure the fundamental component of the system frequency with a reasonable amount of accuracy to ensure secure operation. The relays filtering requirements are dependent on its application. Overcurrent type relays should be designed to operate at the fundamental frequency. Filtering in relays should contain certain characteristics essentially:

- Bandpass response, about the system frequency, because all other components are not of interest.
- DC and ramp rejection to guarantee decaying exponentials are filtered out
- Harmonic attenuation or rejection to limit the effects of non-linearity’s
- Reasonable bandwidth for fast response
- Good transient behaviour
- Simple to design, build manufacture.

Choosing the correct filtering technique based on the application is not enough. It is advisable to test the relays filters response in realistic conditions. Sometimes electromagnetic transient programme type simulation tests are simply not adequate. [19]

2.21 IEEE STD 1036-2010 GUIDE FOR APPLICATION OF SHUNT POWER CAPACITORS

The IEEE STD 1036-2010 provides useful insight into common design requirements and behavioural responses of capacitor banks when connected to the grid. IEEE standards are developed by a board of members whose expertise fall within that particular field. Therefore adopting and implementing these guidelines is often beneficial and often prevents reinventing the wheel. Formulas are used out of the standard to calculate peak inrush currents for single and double bank energizing condition’s and are based on certain assumptions. In the case of chapter 6 which focuses on capacitor bank switching the formulas presented are used to check switchgear current ratings, this is not to say they cannot be adapted for other purposes. The IEEE suggest that if the calculations for the switching devices rating is not exceeded doing the simple calculation with just the reactance a more detailed calculation is not necessary. This appears to be the basis on which they choose to justify the selection of their formulas. [12]
2.22 POINT ON WAVE SWITCHING

The capacitor bank makes use of an Areva RPH2-1SIA0v point on wave switching controller. This controller applies a method of switching known as synchronous switching. The controller has the ability to close each phase or breaker pole independently. It applies its internal logic based on input parameters to attempt closing the poles at a specific required time. However, the device is not perfect and can be influenced by external factors that can affect its operation times. These factors can include:

1. Ambient temperature.
2. Condition and characteristics of arc extinguishing medium.
3. Stored energy (air or hydraulic pressure, spring tension).
4. Control voltages.
5. Number of previous operations
6. Aging effects (lubrication may deteriorate, mechanical parts will wear, corrosion may occur, springs and seals may change their properties, etc.).
7. Intervals between operations (infrequent operations give an uncontrolled time spread).
8. Contact burning (Pre-arcing).
9. Seasonal ambient and environmental effects on the mechanical system (Sea environment, humidity, arctic and desert climates).
10. Contact bounce and contact rebound.

Therefore in some cases during the closing transition of each pole the transitory resultant values are not zero due to staggered switching. The following equation represents the magnitude of current that would be experienced on a per phase basis. [15]

\[ i = \sqrt{2} \times l_{pse} \left[ e^{\sqrt{2} \cos(\theta - \alpha) - (\cos \omega t + \theta - \alpha)} \right] \] (1)

Where \( \theta = \) Angle of switching on the voltage wave \( l_{pse} = \frac{V_m}{(R^2 + \omega^2 L^2)^{\frac{1}{2}}} \) the r.m.s. value of primary symmetrical short circuit current \( Tp = L/R \) is the primary time constant and \( \alpha = \tan^{-1} (\omega L/R) \) is the phase angle difference between voltage and current. Assuming the network predominantly inductive it is preferable for switching to take place on voltage wave when passing through zero. [20]
2.23 CONCLUSION

The purpose behind the literature review was to investigate Eskom’s design and application philosophies used on shunt capacitor bank protection. This includes all apparatus used on a primary and secondary plant level. A review of various phenomena associated with capacitor bank switching was also examined. This was beneficial as it highlighted transient scenarios which are possibly occurring on site. Proper approaches and products using software simulation for transient analysis were also explored and considered. This emphasized the notion that a suitable EMTP type simulation programme is required to investigate the capacitor bank switching phenomenon.

After considering all possible variables which revolve around a successful restricted earth fault protection circuit design. It is clear that there are a few modes of possible failure both in system design and operation. It is desirable that these are addressed before the commissioning of the apparatus takes place to prevent complications. This can be achieved by various techniques. Performing system simulations and fault studies provide insight into system fault levels required for setting calculations. Consulting engineering standard requirement documents usually provide an effective base to implement existing designs from. These can more often than not be reworked and tailor made to meet similar requirements. However each new application should be treated on merit and each new scenario promotes new problems. These problems in some cases fall outside of the design scope and in such cases further action needs to be taken. This may include performing site investigations and research.
3.1 INTRODUCTION

Capacitor bank energizing transients are unique and require a thorough analysis when considering installation of capacitor banks in a power system network. Capacitors banks are often a feasible alternative when compared to synchronous condenser’s but pose their own exclusive challenges. These problems are not new in the field of power system engineering and much research has been conducted in this regard. Bearing this in mind it is good practice to treat each case on merit as each situation’s parameters and conditions are different. Calculations based on system conditions provide valuable information regarding inrush currents and frequencies. Furthermore the values of these calculations can be used to derive settings for protection relays. However it must be appreciated that there is always the possibility that errors in computations may occur causing errors to sieve through the setting calculation process. This is further complicated by the non-linear nature of system components under transient conditions. A sound practice is cross checking calculations with software simulations checking for authenticity.

In addition non-linear circuit elements are difficult to predict during energization and are prone to produce non-sinusoidal signals. These signals when used in electrical protection circuits are used as analogue inputs and are processed by the relay. Ideally the relay is designed to operate off a fundamental system frequency, but this does not discount the behavioural response of the various devices in the circuit when exposed to inputs which are non-sinusoidal in nature. Relay manufactures often cannot test their products under all possible power system conditions. This gives rise to problems manifesting themselves when the devices are put into commission. If one can thoroughly and systematically work through the problematic circuit with its associated parameters and identify possible failure modes a solution can more often than not be found.

Capacitor banks usually consist of groups of single elements. Simplification is required in order to establish a less complex equivalent circuit. In order to simplify the particular circuit numerous equations have to be applied and various calculations performed to develop equivalent impedances. Once specific equivalent impedances are derived inrush currents can be calculated. Furthermore the results of the inrush current calculations can then be used to derive relay setting parameters.

3.2 CAPACITOR BANK CALCULATIONS

As with most spurious relay operation a wise practice is first investigate and validate the settings and calculations applied to derive these operational input parameters. This is necessary as the relay operates off predetermined set values derived from calculations. Both calculations and settings can be subject to human error resulting in unexpected operation. Similarly these calculations are used in later capacitor bank simplified circuit models for software simulation. Basic network reduction theory is applied with the aim of lumping all
the elements together as common components. The following information is found on the nameplate of a single capacitor can.

<table>
<thead>
<tr>
<th>Single Can</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
</tr>
<tr>
<td>Reactive Power</td>
</tr>
<tr>
<td>Nominal Voltage</td>
</tr>
<tr>
<td>Nominal capacitance</td>
</tr>
<tr>
<td>Nominal current</td>
</tr>
</tbody>
</table>

Table 1-1: Parameters for a single capacitor can element found within the shunt capacitor bank.

Capacitor Banks consist of multiple cans interconnected by various methods. This normally includes series and parallel branches. The reason behind this is for ease of installation and replacement in the event of unit failure. The Structure of the bank is shown below in figure 1.14.

![Shunt capacitor bank arrangement](image)

**Shunt capacitor bank arrangement:**

- Configuration: Single Star Earthed
- Between phases: ungrounded single wye
- Number of units in series: 16
- Strings per phase: 6
- Number of CAP. Elements in parallel per can: 3
- Number of CAP. Elements in series per can: 9

Figure 1.14: Layout of the bank is shown above showing all individual elements and interconnections.
To calculate the overall bank capacitance the parameters are lumped together as follows. A phase string consists of a number of units in series. Each phase is made of 16 elements in 1 string of which there are 6 strings in each phase. To aid the calculation the capacitance value is converted to an equivalent impedance value at a system frequency of 50Hz.

\[ X_c = \frac{1}{2\pi \times f \times c} \]  

(2)

\[ X_c = 626.348 \text{Ω for a single can} \]

With 16 cans in series

\[ 16 \times 626.348 = 10021.568 \]

And 6 strings in parallel

\[ (\frac{1}{10021.568} \times 6)^{-1} = 1670.2613 \text{Ω for a phase} \]

The impedance for the earthing capacitors on a phase is calculated in the same manner. Data for the earthing capacitors is as follows:

<table>
<thead>
<tr>
<th>Single Can</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
</tr>
<tr>
<td>Westingscorp</td>
</tr>
<tr>
<td>Reactive Power</td>
</tr>
<tr>
<td>167kVAr</td>
</tr>
<tr>
<td>Nominal Voltage</td>
</tr>
<tr>
<td>825V</td>
</tr>
<tr>
<td>Nominal capacitance</td>
</tr>
<tr>
<td>781uF</td>
</tr>
</tbody>
</table>

Table 1-2: Parameters for a single earthing capacitor can element found within the shunt capacitor bank.

There are 4 of these capacitor cans in parallel for each phase between the neutral and star points of the bank. Impedance for the earthing capacitors is calculated below are 50Hz.

\[ X_{ce} = -j \frac{1}{2\pi \times f \times c} \]  

(3)

\[ X_{ce} = 4.075 \text{Ω for a single can} \]

And 4 cans in Parallel

\[ (\frac{1}{4.075} \times 4)^{-1} = -j 1.019 \text{Ω for a phase} \]

It is noticeable that this value is significantly smaller than the total phase capacitance. Generally these are used to provide a negligible impedance at nominal current and frequency thus elevating the neutral point of the bank. This is a requirement for the unbalance protection which measures the unbalance current flowing in the neutral. If this impedance was negated the current would flow into the earth mat. A resistor is connected in parallel with the earthing capacitors and is rated 100 Ω and if included in the calculation yields the following:

\[ Z_{cer} = \frac{X_c \times R}{X_c + R} \]  

(4)
$Z_{cer} = 0.02 - 1.019j$

Furthermore a surge inductor is present on each phase. This is located between the phase capacitors and neutral point of the bank. The information for the inductor is as follows:

<table>
<thead>
<tr>
<th>Filter Reactor</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>Areva Brazil</td>
</tr>
<tr>
<td>Nominal Inductance</td>
<td>1.2mH</td>
</tr>
<tr>
<td>Nominal Current</td>
<td>200A</td>
</tr>
</tbody>
</table>

Table 1-3: Parameters for a single earthing capacitor can element found within the shunt capacitor bank.

The impedance for the inductor is calculated as follows at 50Hz:

$$X_L = 2 \times \pi \times f \times L$$

$$X_L = 0.376 \Omega$$

With these values it is now possible to calculate the total impedance of one phase. All the elements are in series so one simply needs to add them together as follows:

$$Z_t = -jX_{c\ phase} + Z_{cer} + jX_L$$

$$Z_t = -j 1670.2613 \Omega + (0.02 \Omega - j 1.019 \Omega) + j 0.376 \Omega$$

$$Z_t = 0.02 - j 1670.904 \Omega$$

The value of R has been omitted in further calculations because of small magnitude and only the $X_c$ component considered. Converting this to an equivalent capacitance for one whole phase.

$$C_{eq} = \frac{1}{2\pi f \times X_t}$$

$$C_{eq} = \frac{1}{2\pi \times f \times 1670.904}$$

$$C_{eq} = 1.905 \mu F / per\ phase$$

Full load current of the capacitor bank with $V_{line} = 400$ kV.

$$I_{full\ load} = \frac{V_{line}}{\sqrt{3}} \times \frac{1}{X_t}$$

$$I_{full\ load} = 138.15 \ A$$

These are the steady state operating conditions.
3.2.1 Capacitor bank inrush Calculations

Information for the Capacitor Bank obtained from the manufacturer and site is proved useful in calculating steady state values of the capacitor bank. However, the underlying problem occurs during switching transient events. For these calculations further information is required. Using network reduction theory a Thévenin equivalent circuit is created for the network. The equivalent circuit contains an equivalent source impedance and voltage.

![Figure 1.15 Equivalent Source model required to be derived for inrush calculations.](image)

3.2.1.1 Source Impedance

The system source in the model is modelled as an ideal voltage source behind a system equivalent impedance. The impedance used in the model is derived from Digsilent Power factory. Both positive and zero sequence inductance and resistance are included in system source with angles incorporated. The voltage source magnitude parameter is set to be 400 kV before capacitor energization. This magnitude varies real-time in the station and is dependent upon system loading and operating conditions. Therefore, these parameters will have to be reassessed when system conditions change. Similarly this also applies to system impedance values. Equivalent circuit parameters are derived from a network model of the Eskom transmission grid. Eskom’s transmission network model is constructed in Digsilent Powerfactory which is the preferred software of the utility system operator. Equivalent source and source impedance parameters are derived from Digsilent by applying a symmetrical three phase fault on the 400kV busbar which the capacitor bank is connected to.
After running the simulation the following results were obtained shown in table 1-4. Two fault types were applied to the busbar where the capacitor banks are connected to a bolted three phase fault and a single phase earth fault. The faults were applied using IEC 60909 in Short Circuit Calculation function. Zero Fault Impedance for the earth fault condition was deselected as the earth mat is the local earth return path in the substation. The values derived above are used for future calculation pertaining to inrush currents.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ss}$</td>
<td>17296 A</td>
</tr>
<tr>
<td>$Sk_{ss}$</td>
<td>11983.106 MVA</td>
</tr>
<tr>
<td>$R$</td>
<td>3.33 $\Omega$</td>
</tr>
<tr>
<td>$X$</td>
<td>13.057 $\Omega$</td>
</tr>
<tr>
<td>$Z$</td>
<td>13.539 $\Omega$</td>
</tr>
<tr>
<td>$\cos \theta$</td>
<td>74.663</td>
</tr>
<tr>
<td>$\frac{Z}{X}$ ratio</td>
<td>19.48</td>
</tr>
</tbody>
</table>

Table 1-4: Parameters sourced from Digsilent Power Factory for three and single phase bolted earth faults on the local 400kV busbars at Hydra Substation.
3.2.2 Single Bank Energizing

While energizing a single bank the source impedance $X_s$ is of particular interest. This directly effects the characteristics and magnitude of the inrush current during single bank energizing. With the availability of the source impedance further calculations can be done. The following circuit represents a single capacitor bank energizing scenario. The current flowing into $C_b$ is only limited by $L_s$ and $R_s$.

![Circuit Diagram](image)

Figure 1.17 Inserting equivalent parameters for the shunt capacitor bank into the source impedance model to calculate single bank inrush currents.

$$L_s = \frac{X_s}{2\pi f}$$

\[= \frac{13.057}{2\pi \times 50} = 42.9 \text{ mH} \tag{9}\]

We can now see that we have a second order differential equation and can apply Kirchhoff’s voltage law to set up an equation for the circuit.

$$V_s = V_{Ls} + V_{C_b} + V_{Rs} \tag{10}$$

Energy through a capacitor or inductor cannot change instantaneously. Second order circuits have two energy storage devices, in this specific circuit they are the inductor and capacitor. Therefore an equation is required to describe the circuit from a time variant perspective. Moreover we know that for transient analysis $L$, $C$ and $R$ components can be expressed as follows:

$$L_s \frac{di}{dt} \tag{11}$$

$$i_{C_b} = \frac{1}{C} \int i \, dt \tag{12}$$

$$V_{Rs} = R_s \tag{13}$$

This leads to

$$V_s \sin (\omega t + \phi) = \frac{d^2i}{dt^2} + \frac{1}{LC} i + \frac{R}{L} \frac{di}{dt} + Vc(0) \tag{14}$$

To obtain the natural response of the circuit a homogenous differential equation will need to be solved and equated to zero forcing an initial condition. The next step would be the calculation of the current through the
inductor at \( t=0 \) and voltage across the capacitor at \( t=0 \) as well as the variable which we are solving for \( i(t) \). This provides the characteristic equation and offers variables such as damping ratio, damping factor and the roots. After this phase it is possible to determine the case of the equation which will allow progression to the next step.

\[
L = 42.9 \text{ mH} \quad C = 1.91 \text{ uF} \quad R = 3.33 \Omega
\]

\[
0 = \frac{d^2i}{dt^2} + \frac{1}{LC}i + \frac{R}{L} \frac{di}{dt}
\]

From this point the solution can be obtained using differential equations as stated before but this method is tedious. A common practice used to verify switch gear ratings for capacitor banks is to use the IEEE Std 1036-2010 a guide for use capacitors on the power system network. These equations are adopted here to calculate worst case inrush currents. The worst possible current that will occur and will transpire when both the 50Hz current and the resonant current peak at the same time. However due to the resistance in the circuit the oscillation will eventually settle to the steady state value calculated as the particular solution. The damping factor shown below where \( \alpha \) represents the neper frequency or alternatively the attenuation and indicates how quickly the transient will subside. In addition \( \omega \) is the angular resonant frequency. The damping factor is calculated as follows:

\[
\zeta = \frac{\alpha}{\omega} \quad (15)
\]

Furthermore \( \alpha \) can be calculated as follows

\[
\alpha = -\left(\frac{R}{2L}\right)
\]

\[
\alpha = -\frac{3.33}{2(42.9 \text{ mH})} = -38
\]

Similarly the current will be maximum when the circuit is driven at its resonant frequency, it is possible to calculate the resonant frequency of the circuit.

\[
\omega = \frac{1}{\sqrt{LC}} \quad (16)
\]

\[
= \frac{1}{\sqrt{42.9 \text{ mH} \times 1.91 \text{ uF}}} = 3498.951 \text{ rad}
\]

But

\[
f_c = \frac{\omega}{2\pi} \quad (17)
\]

\[
= \frac{3498.951}{2\pi} = 556.87 \text{ Hz}
\]
And solving for the damping factor

\[ \zeta = \frac{38.81}{3498.951} \]
\[ \zeta = 0.0111 \]

The IEEE Std 1036-2010 Guide for Application of Shunt Power Capacitors recommends the use of the following formula to calculate the magnitude of \( I_{\text{peak max}} \) this equation negates the effect of damping in the circuit. Without the consideration of damping the circuit is presumed to be loss-free. This is due to the fact that there is no dissipative element present. All realistic circuits have losses present and is normally in the form of circuit resistance and iron losses.

\[
I_{\text{peak max}} = 1000 \times V_{\text{LL}} \sqrt{\frac{2}{3}} \times \sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}}
\]  \quad (18)

Where \( C_{\text{eq}} \) is the effective capacitance of the capacitor bank (in farads).
Similarly \( L_{\text{eq}} \) is the effective inductance of the source (in henries).

\[
I_{\text{peak max}} = 1000 \times V_{\text{LL}} \sqrt{\frac{2}{3}} \times \sqrt{\frac{1.904 \mu F}{42.9 mH}}
\]
\[ I_{\text{peak max}} = 2175.80 \text{ A} \]
\[ I_{\text{rms max}} = 1538.522 \text{ A} \]
3.2.3 Double Bank Energizing

When intending on energizing a capacitor bank in close proximity to a previously energized capacitor bank, additional considerations need to be accounted for. This condition will present a high-frequency inrush current which will flow between the two capacitor banks being energized Cb1 and Cb2. Nevertheless unlike single bank energizing scenarios the limiting inductance is not the system inductance Ls but rather the inductance between the two capacitor banks Lb. Logically system inductance is quite large whereas the inductance between the two banks will be quite small. Therefore the magnitude and frequency of this inrush current will be of a much higher magnitude and frequency than the inrush current of an single capacitor bank.

![Source impedance model to calculate double bank inrush currents.](image)

Firstly we need to consider the transient flowing between the two capacitors. To do this we need to consider the combination of the two capacitors in parallel.

$$L_b = 2. mH \quad C_{b1} and \quad C_{b2} = 1.91 \ \mu F \quad R_s = 3.3 \ \Omega \quad L_s = 42.9 \ mH$$

$$C_{eq} = \frac{C_{b1} \times C_{b2}}{C_{b1} + C_{b2}}$$

$$C_{eq} = 0.95 \ \mu F$$

Similarly the frequency of the transient inrush current between the two capacitor banks can be calculated as follows:

$$\omega = \frac{1}{\sqrt{L_b C_{eq}}}$$

$$= \frac{1}{\sqrt{2.4 \ mH \times 0.95 \ \mu F}}$$

$$= 20942.695 \ \text{rad}$$

But

$$f_{c1,c2} = \frac{\omega}{2 \pi} = \frac{3498.951}{2 \pi} = 533.13 \ \text{Hz}$$
\[ T_c = \frac{1}{f_c} = 0.30 \text{ms} \]

Likewise the frequency of the transient inrush current between the two capacitor banks and the source can be calculated as follows:

\[ \omega = \frac{1}{\sqrt{L_s(C_{1} + C_{2})}} = \frac{1}{\sqrt{42.9 \text{ mH} \times 3.884 \text{ mF}}} = 2438.531 \text{ rad} \]

And

\[ f_s = \frac{\omega}{2\pi} = \frac{3498.951}{2\pi} = 558.104 \text{ Hz} \]

\[ T_c = \frac{1}{f_c} = 2.57 \text{ms} \]

The first bank will has an initial charge already of \( V_p \) but the second bank is uncharged at OV, therefore an oscillating voltage will exist flow between the two banks and the source. This is somewhat smaller than the current flowing between the two banks and is quickly dampened out by the source resistance. Its effects are often ignored for double bank energizing. As seen before the IEEE Std 1036-2010 Guide for Application of Shunt Power Capacitors recommends the use of the following formula to calculate the magnitude of \( I_{\text{peak max}} \) for double bank energizing conditions.

Similarly this equation negates the effect of damping in the circuit.

\[ I_{\text{peak max}} = 1000 \times V_{LL} \times \frac{2}{3} \times \sqrt{\frac{C_{eq}}{L_{eq}}} \]  

(20)

Where \( C_{eq} \) is the effective capacitance of both banks in the series (in farads).

\[ C_{eq} = \frac{C_{b1} \times C_{b2}}{C_{b1} + C_{b2}} \]

Similarly \( L_{eq} \) is the effective inductance between the two capacitor banks (in henries). Furthermore this includes the inductance of the two shunt reactors for both the banks.

\[ I_{\text{peak max}} = 1000 \times V_{LL} \times \frac{2}{3} \times \sqrt{\frac{0.952uF}{2.4mH}} \]

\[ I_{\text{peak max}} = 6504.699A \]

\[ I_{\text{rms max}} = 4599.51A \]

The calculations performed above are used for further calculations in determining the correct settings for the relay. It is important to note that system conditions are dynamic and changes in parameters occur dependent on system configurations. Each situation must be calculated on based on the particular network configuration. The IEEE calculations are a somewhat simplified analysis they
choose to consider the source to be a DC voltage. This is appropriate in the case of the IEEE standard as they favour the circuit to be analysed as an equivalent LC network. To be less conservative a software simulation is required with resistance included to indicate maximum peak inrush conditions.
3.3 SETTING CALCULATIONS FOR REF RELAY

A selected voltage setting on the relay should exceed the voltage across the relay terminals for inrush current conditions. IEEE standard introduces equations that are beneficial in the calculation of capacitor bank inrush currents [4]. These calculations are important as they indicate what the magnitude of the maximum theoretical current in the circuit will be under energizing conditions. This is of particular importance as it can directly influence protection performance. Nominal current in the bank was calculated as shown in the previous chapter. Peak inrush current for the energizing of a single or parallel SCB without damping in Amperes is calculated in eq (18) and eq (20). In practical circuits, it will be about 90% of this value. The following data below in table 1-5 is required to perform the calculations along with the calculated values for inrush currents calculated previously.

<table>
<thead>
<tr>
<th>Single Bank Inrush Current</th>
<th>2157.80A peak or 1538.522A rms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Double Bank Inrush Current</td>
<td>6504.699A peak or 4599.51A rms</td>
</tr>
<tr>
<td>Kneepoint voltage Neutral CT</td>
<td>445.01V @ 24.56mA</td>
</tr>
<tr>
<td>Kneepoint voltage Red Phase CT</td>
<td>2640V @ 10.5mA</td>
</tr>
<tr>
<td>Kneepoint voltage White Phase CT</td>
<td>2640V @ 10.7mA</td>
</tr>
<tr>
<td>Kneepoint voltage Blue Phase CT</td>
<td>2640V @ 10.6mA</td>
</tr>
<tr>
<td>Lead Resistance ($R_{LEAD}$)</td>
<td>2.5 Ω (measured on site)</td>
</tr>
<tr>
<td>CT secondary Resistance ($R_{CT}$)</td>
<td>1.6 Ω (measure on site)</td>
</tr>
<tr>
<td>Varistor Constant K</td>
<td>320</td>
</tr>
</tbody>
</table>

Table 1-5: Protection circuit parameters required form setting calculations.

Single bank energising current transients of 5 – 20 p.u have been experienced. Furthermore if another SCB bank is energized in close proximity to a previously energized capacitor bank further considerations for inrush current need to be addressed. In the case of back to back energizing transient currents of 40 - 100 p.u have been experienced. The magnitude and frequency of this inrush current is, therefore, much higher than the inrush of an isolated capacitor bank [5]. This multiplication factor figure for inrush conditions is not found in the relay manual for SCB applications as its application is intended for classical REF applications normally found power transformers. The setting voltage is related to the inrush current as shown in the formula below:

$$V_{eff} > \frac{i_{inrush}}{CR_{ratio}} \times (R_{CT} + 2 \times R_{LEAD})$$  \hspace{1cm} (21)

Where $V_{eff}$ is the setting voltage, required to exceed voltage across relay during inrush. As seen from eq (21) the assumption of $i_{inrush}$ will directly effect the value of the required setting voltage and affects further calculations. Furthermore this selected factor does not cater for double bank energizing conditions. Therefore $V_{eff}$ for single bank scenario is calculated using IEEE recommended standard of inrush current from eq(18).
\[ V_{\text{eff}} > \frac{153.522}{400} \times (1.6\Omega + 5\Omega) \]
\[ V_{\text{eff}} > 25.38 \, V \]

In addition \( V_{\text{eff}} \) for double bank scenario is calculated using current magnitude values in eq(20) derived from the IEEE recommended standard. Therefore for a double bank the calculation is presented below.

\[ V_{\text{eff}} > \frac{4599.51A}{400} \times (1.6\Omega + 5\Omega) \]
\[ V_{\text{eff}} > 75.89 \, V \]

It must be noted that these are worst case scenarios where closing will occur at peak on the voltage waveform. According to the relay manual there are various predefined voltage settings available. These are as follows:

<table>
<thead>
<tr>
<th>Setting Voltage ( V_R ) in volts</th>
<th>24</th>
<th>48</th>
<th>72</th>
<th>96</th>
<th>120</th>
<th>144</th>
<th>168</th>
<th>192</th>
<th>216</th>
<th>240</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relay current ( I_R ) (including varistor) in mA</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>22</td>
<td>22</td>
<td>23</td>
<td>25</td>
<td>26</td>
<td>28</td>
<td>30</td>
</tr>
</tbody>
</table>

Table 1-6: Range of settings available for selection for the restricted earth fault relay.

From the table 1-6 above the selectable setting should be higher than that calculated. The setting for single bank energizing conditions will be 48V and for double bank energizing conditions 96V. A recommendation for the relay manual is that the kneepoint voltage of the current transformer must be at least twice relay setting voltage to ensure reliable operation. In this case it equates to 48V which is substantially lower than the kneepoint of the current transformers in use. [6]

Current transformer magnetization curve characteristics are now required to calculate the current drawn for the \( V_{\text{eff}} \) value of voltage. The current transformers test results are used to validate the nameplate data. Currents used for the magnetization curve for the phase ct’s were taken as an average of all three ct’s as the kneepoint currents only differ by 1mA.

Single bank
\[ I_{ct\, \text{phase}} = V_{\text{eff}} \times \left( \frac{I_{\text{knee\ phase\ ct}}}{V_{\text{knee\ phase\ ct}}} \right) \]  
\[ I_{ct\, \text{phase}} = 25.38V \times \left( \frac{10.6mA}{2640V} \right) \times \frac{2640}{400} \]
\[ I_{ct\, \text{phase}} = 672\mu A \]
\[ I_{ct\, \text{neutral}} = V_{\text{eff}} \times \left( \frac{I_{\text{knee\ neutral\ ct}}}{V_{\text{knee\ neutral\ ct}}} \right) \]
\[ I_{ct\, \text{neutral}} = 25.38V \times \left( \frac{24.56mA}{445.01} \right) \]
\( I_{ct\ neutral} = 1.4mA \)

Double Bank

\[
I_{ct\ phase} = V_{eff} \times \left( \frac{I_{knee\ phase\ ct}}{V_{knee\ phase\ ct}} \right) \\
I_{ct\ phase} = 75.89V \times \left( \frac{10.6mA}{2640V} \right) \times \frac{2640}{400} \\
I_{ct\ phase} = 2mA
\]

\[
I_{ct\ neutral} = V_{eff} \times \left( \frac{I_{knee\ neutral\ ct}}{V_{knee\ neutral\ ct}} \right) \\
I_{ct\ neutral} = 75.89V \times \left( \frac{24.56mA}{445.01} \right) \\
I_{ct\ neutral} = 4.1mA
\]

Where \( B \) and \( K \) are constants attributed to the varistor of a certain type and \( K = 320 \) and \( B = 0.25 \). This is obtained from the relay manual [6]. Settings where calculated using the above formula.

\[ V_{\text{varistor}} = K \times I^B \] (23)

Which can be simplified to:

\[ I_{\text{varistor}} = \left( \frac{V_S}{K} \right)^\frac{1}{B} \]

For single bank energizing selected \( V_S \) is 48V.

\[ I_{\text{varistor}} = \left( \frac{48V}{320} \right)^\frac{1}{0.25} \]
\[ I_{\text{varistor}} = 506\mu A \]

For double bank energizing selected \( V_S \) is 96V.

\[ I_{\text{varistor}} = \left( \frac{96V}{320} \right)^\frac{1}{0.25} \]
\[ I_{\text{varistor}} = 8.1mA \]

The effective primary current \( I_{eff} \) at a particular setting equals the magnetizing current drawn by the four current transformers at the voltage setting. These currents are obtained from the magnetization curve using the voltage setting and the current drawn by the varistor at the calculated voltage setting as shown above.

Single Bank primary current required for operation can be calculated as follows:

\[ I_{eff} = [3 \times I_{ct\ phases} + I_{ct\ neutral} + I_{relay} + I_{var}] \times CT\ ratio \] (24)
\[ I_{eff} = [3 \times 672\mu A + 1.4mA + 20mA + 506\mu A] \times 400 \]
\[ I_{eff} = 9.56 \text{ primary} \]

Double Bank primary current required for operation can be calculated as follows
With this in mind the REF coverage of the bank is now calculated, this will determined how much sensitivity the REF protection will offer for faults within the capacitor bank. Consequently if the fault occurs close to the neutral point it may be difficult to detect as a small impedance change will occur in the bank producing a small current increase.

![Figure 1.19 Single phase equivalent circuit simplification method for calculating equivalent phase impedance in the event of an earth fault.](image)

In order to calculate the current flow for an earth fault scenario within a string an equivalent circuit is required. There are obviously many locations that an earth fault can occur within the bank. However the further away from the neutral point the fault occurs the greater the fault current that will flow. The phase configuration shown in figure 1.14 is simplified by deriving and combining equivalent values of capacitances encompassed within the coloured blocks i.e. A is combined with B and C is combined with D. With a bank element having a

\[
C_{1} = 5.082 \text{uF} \quad \text{and} \quad C_{5} = 781 \text{uF}:
\]

A is calculated as follows:

\[
C_{4} = 3 \times C_{1} = 3 \times 5.082 \text{uF} = 15.246 \text{uF}.
\]

B is calculated as follows:

\[
C_{1} = 5.082 \text{uF}.
\]

C is calculated as follows:

\[
C_{16} = (5.082^{-1} \times 16)^{-1} = 0.317 \text{uF}.
\]

\[
C_{5} = (0.317 \times 5) = 1.588 \text{uF}.
\]

D is calculated as follows:

\[
C_{15} = (5.082^{-1} \times 15)^{-1} = 0.338 \text{uF}.
\]
If it is a bolted fault A and B are no longer included in the circuit and total equivalent capacitance will be C in parallel with D.

Capacitance \( C \) in parallel with \( D = 1.588uF + 0.338uF = 1.926uF \).

Therefore comparing this capacitance with the \( \text{Capacitance of a healthy phase} = 1.905uF \) it can be seen that there is only an \( 0.021uF \) increase of capacitance on the unhealthy phase. There is a general formula according to IEEE Std 1036-2010 shown below that can be applied in a string of capacitance to detect failure.

\[
C \ (\text{faulted string}) = \frac{n}{S-n}
\]

Where \( n \) would be the number of failed elements in the series sting and \( S \) the total number of elements in the string. Thus placing the earth fault \( n \) places from the neutral would effectively render the elements below inoperable. The value of this equation produces a ratio that must be multiplied by the total healthy string capacitance. The answer will yield the increase in capacitance value of the string. In this case if we choose an element failure at element number 1 from the bank the above formula yields the following result.

\[
C \ (\text{faulted string}) = \frac{1}{16-1}
\]

Now to achieve equivalent increase we perform the following:

\[
C \ (\text{faulted string}) \times \text{Healthy String Capacitance}
\]

\[
0.317uF \times \frac{1}{15} = 0.021uF
\]

The calculation above can be used to simplify calculations of equivalent string impedances when trying to determine earth fault current flow. Assuming a bolted earth fault with no arc resistance on one phase within the string at different points as shown in figure 1.19 the following values for fault earth fault currents are calculated. As an earth fault location moves from the star point of the bank up to the can before the busbar voltage the fault magnitude increases. This will also be dependent on the system voltage at the time of the fault.
Table 1-7: The following table illustrates the reduction in phase impedance for earth fault locations at different points in a single string.

<table>
<thead>
<tr>
<th>Earth Fault Location in Bank String</th>
<th>Equivalent String Impedance in Ω</th>
<th>Equivalent Phase Impedance in Ω</th>
<th>Calculated Phase Fault Current in Amps</th>
<th>Simulation phase fault current in Amps</th>
<th>% error in Calculated vs Simulation</th>
<th>Calculated Resultant Current in Amps</th>
<th>Simulation Resultant Current in Amps</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 9395.492</td>
<td>1651.954665</td>
<td>139.7980905</td>
<td>140.89</td>
<td>1.007810618</td>
<td>2.74</td>
<td>1.536243</td>
<td></td>
</tr>
<tr>
<td>2 8769.126</td>
<td>1631.465305</td>
<td>141.5537965</td>
<td>142.68</td>
<td>1.007956011</td>
<td>4.53</td>
<td>3.291949</td>
<td></td>
</tr>
<tr>
<td>3 8142.76</td>
<td>1608.446394</td>
<td>143.5796111</td>
<td>144.735</td>
<td>1.008047026</td>
<td>6.585</td>
<td>5.317763</td>
<td></td>
</tr>
<tr>
<td>4 7516.394</td>
<td>1582.398679</td>
<td>145.9430615</td>
<td>147.133</td>
<td>1.008153443</td>
<td>8.983</td>
<td>7.681214</td>
<td></td>
</tr>
<tr>
<td>5 6890.028</td>
<td>1552.682272</td>
<td>148.7362301</td>
<td>149.967</td>
<td>1.008274849</td>
<td>11.817</td>
<td>10.47438</td>
<td></td>
</tr>
<tr>
<td>6 6263.661</td>
<td>1518.463379</td>
<td>152.0880325</td>
<td>153.369</td>
<td>1.00842254</td>
<td>15.219</td>
<td>13.82618</td>
<td></td>
</tr>
<tr>
<td>7 5637.295</td>
<td>1478.634831</td>
<td>156.1846798</td>
<td>157.528</td>
<td>1.008600845</td>
<td>19.378</td>
<td>17.92283</td>
<td></td>
</tr>
<tr>
<td>8 5010.929</td>
<td>1431.690403</td>
<td>161.305489</td>
<td>162.729</td>
<td>1.008824938</td>
<td>24.579</td>
<td>23.04364</td>
<td></td>
</tr>
<tr>
<td>9 4384.563</td>
<td>1375.549178</td>
<td>167.8893865</td>
<td>169.42</td>
<td>1.009116797</td>
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<td>29.62754</td>
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</tr>
<tr>
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<td>1307.198909</td>
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<tr>
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<td>1222.177841</td>
<td>188.9578586</td>
<td>190.855</td>
<td>1.010040024</td>
<td>52.705</td>
<td>50.69601</td>
<td></td>
</tr>
<tr>
<td>12 2505.465</td>
<td>1113.539811</td>
<td>207.3927716</td>
<td>209.641</td>
<td>1.010840438</td>
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</tr>
<tr>
<td>13 1879.098</td>
<td>969.8572548</td>
<td>238.1176267</td>
<td>241.081</td>
<td>1.012444998</td>
<td>102.931</td>
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</tr>
<tr>
<td>14 1252.732</td>
<td>770.9121769</td>
<td>299.5673368</td>
<td>304.015</td>
<td>1.014846957</td>
<td>165.865</td>
<td>161.3055</td>
<td></td>
</tr>
<tr>
<td>15 626.3661</td>
<td>477.2313476</td>
<td>483.9164671</td>
<td>494.991</td>
<td>1.022885216</td>
<td>356.841</td>
<td>345.6546</td>
<td></td>
</tr>
</tbody>
</table>

It can be seen from eq (24) that the setting of 48V requires an $I_{eff} = 9.56 \text{ primary}$, when comparing this value to the highlighted column in table 1-7 it can thus be seen that the current required to operate the relay will be sufficient when the fault occurs from element 4 to element 15. Similarly a setting of 96V requires an $I_{eff} = 15.28 \text{ primary}$ will provide earth fault detection form element 5 onwards to element 15.
3.4 CURRENT TRANSFORMER PERFORMANCE

A protection scheme’s reliable operation is also fundamentally dependent on the protection relays analogue input sources which are provided by the current or voltage transformers. A requirement for older type REF protection is the matching of current transformer characteristics. Matching of current transformers can normally be achieved by using CT’s with the same specifications. This is normally performed to ensure limited spill current during heavy through fault condition. For the circuit under instigation the current transformers differ. The neutral current transformer is of a different manufacturer and type as compared to phase CT’s. In order to compare the neutral CT’s performance with the phase CT’s a magnetization curve plot was done.

Cognises must be taken that the manufacturer defines the nominal knee point on the CT based on the highest tap. The knee point is defined as the point on the magnetizing curve where a 10% increase in the voltage corresponds to a 50% increase in the magnetizing current. The ratio in use on the neutral CT is 400/1 and the knee point voltage and current can be used directly from the nameplate. However for the phase CT’s the knee point voltage and current is provided at a full ratio of 2400/1. Similarly if the required ratio is known the corresponding knee point can be directly calculated at a lower tap. The knee point voltage will be proportionally lower than nominal knee point voltage and should vary linearly as a function of tap ratio.

![CT Burden comparison CTR400:1](image)

Figure 1.20 Current transformer burden comparisons for the CT’s used in the restricted earth fault circuit.

The results of the burden plot in figure 1.20 show that there are slight differences in all the current transformers used in the REF circuit. Under balanced conditions there will be a slight spill current flowing through the circuit due to these inaccuracies. The particular knee points from the CT manufactures nameplates can be seen above in table 1-5. It must be mentioned that the test set used for testing and obtaining the magnetization curves is only rated up to 2 kV. Therefore it could not derive the knee point on the full ratio of 2400:1 for the phase post type current transformers. This does not pose a problem as the setting falls sufficiently within the recommended specification in term of the magnetization curve parameters. It can be seen from figure 1.20 that the current transformers magnetizing impedances differ from each other. Satisfactory operation is not attainable simply on matching the current transformers, as unbalance is also caused by the nonlinearity of the excitation characteristics.
3.5 ENERGIZING RECORDINGS

Due to the fact that there are no fault recording capabilities on the current protection scheme, a digital fault recording was taken during the energizing of the SCB. This included the respective voltages and currents for the bay. Meanwhile, another important consideration is the recorder sampling frequency. Sampling frequency rates used for recording purposes are selected based on the required power system phenomenon that is being investigated. The Digital Fault Recorder (DFR) used to take the recordings was an Omicron 356 test set used in conjunction with Omicron Enerlyser software. Two switching scenarios are conducted, firstly a single bank is energized and measurement made and secondly with the bank now in service the opposing bank is energized. During the second case both measurements are made on the two capacitor banks.

Figure 1.21: An Omicron CMC356 Test Set connected to the secondary instrumentation circuits within the Capacitor bank protection panel.
Two scenarios are validated, firstly a single bank is energized and measurement made and secondly with the bank now in service the opposing bank is energized. It must be appreciated that the sampling rate chosen to execute the recording is of great importance. The sampling rate will affect the performance of the relay filter when played back through the test set as a Comtrade file. The recording frequency chosen for the recordings was 9 kHz which is more than adequate to record the worst case transient occurrence. In figure 1.22 shows that a record of quality depends on the sample per cycle. The higher the resolution, the better the data quality for record. [21]

![Figure 1.22: Red block waveform indicates a digital representation of the analogue waveform in the background.](image)

The Omicron Enerlyser software has a full set of multifunctional recording suites. Of these the transient recording module was used. The inputs into the DFR consisted of system voltage and bay current. Current recordings are taken using an external type clip on current transformer, the Omicron C-Probe 1 current clamp. Clip on type CT’s are preferable as they are non-invasive and do not disturb the commissioned CT circuits. Voltage measurements were taken from secondary busbar VT circuits.

The Omicron 356 has 10 multifunctional programmable analogue input channels. Accurate configuration of these channels is essential in obtaining an accurate result. Therefore it is required that correct programming of voltage and current inputs is undertaken. The inputs are calibrated based on the secondary circuit types and ratios being recorded.

![Figure 1.23: Enerlyser software setup showing the configurations used to record the current and voltage inputs into the unit.](image)
The fault recording is saved in a Comtrade file format. The Comtrade file format has been standardised by the IEEE and is the file format of choice. Triggering of the recorder is achieved by setting a current threshold level. This ensures that when the capacitor bank is energized the recording will initiate recording soon as the threshold is exceeded i.e. when current starts to flow into the bank. The threshold was set to 50mA with a pre trigger length of 2 seconds. The pre trigger length is the buffer which the recorder runs to capture pre-fault conditions. The post-fault recording length was set to 8s. The total recording time of the DFR is dependent on the sampling frequency resolution chosen. Higher frequencies require more data sampling points which in turn shortens available recording time.

![Enerlyser software showing configuration of sampling frequency and trigger thresholds.](image)

Figure 1.24: Enerlyser software showing configuration of sampling frequency and trigger thresholds.
3.5.1 SCENARIO 1: SINGLE BANK INRUSH SITE RECORDINGS

The single line diagram in figure 1.25 shows the basic outline of an equivalent circuit and at what specific location the recordings are made. The recording is configured in such a manner as to capture both busbar voltages and currents as well as the voltage across the restricted earth fault relay. Two energizing transient scenarios are recorded. Firstly energizing capacitor bank 11, and in turn capacitor bank 12. For these recordings one bank will remain out of service whilst the other is energized.

Figure 1.25. First scenario single bank energizing was recorded for the network configuration above.

The recorded voltages are shown in figure 1.26 from the local busbars which the capacitor banks are connected too. The voltages inputs of the recorder are connected to the secondary circuits of the voltage transformers (VT). The recorded value is dependent on the ratio of the primary to secondary voltage ratio of the VT. In this case the ratio is 400kV/110V. Furthermore the voltages shown in figure 1.26 are required by the point onto wave switching controller to initiate breaker pole closing.

Figure 1.26: Busbar voltages on 400kV busbar recorded whilst energising a single 400kV shunt capacitor bank.

The phase currents are recorded from current transformers connected in each phase on the capacitor bank, as well as the common neutral star point current transformer. The currents pass through the protection circuit and a
voltage is produced as result of the secondary circuit’s impedance. Upon closer inspection of the voltage and currents it is apparent that there is a slight time delay between the zero point on the voltage wave and the onset of current flow. This means that by the time the breaker pole is closing on that particular phase the voltage across the phase bank is no longer at zero. The time will vary based on numerous external factors already discussed.

Figure 1.27: Recorded phase current whist energising 95MVAR 400kV shunt capacitor bank 11.

The current producing the voltage will contain slight inaccuracies when compared to the primary current flowing in the circuit. Consequently this is caused by slight inaccuracies in the current transformers design parameters. Similarly the recording will also contain slight deviations resulting for measurement equipment tolerances. The three distinct spikes coincide with the closing of the breaker poles controlled by the point on wave controller.

Figure 1.28: Recorded voltage waveform during switching appearing across restricted earth fault relay on capacitor bank 11.

One can see that the resultant voltage shown in figure 1.28 which appears across the relay element is a result of the sum of the all the phase and neutral currents. The currents pass through the protection circuit and a voltage is
produced as result of the circuit’s impedance. Upon closer inspection it can be seen that there is a slight time delay between the zero point on the voltage wave and the onset of current flow. Similarly this time will vary based on numerous external factors already discussed.

The bar harmonic analysis of this voltage wave form is shown in figure 1.29. It indicates that the voltage appearing across the relays input terminals is rich in harmonics. It is these harmonics that are of particular interest when testing the response of the restricted earth fault relay. In addition these harmonics can be attributed to the characteristics of energizing capacitor banks.

In order to try and establish what the highest voltage that would appear across the REF relay would be during single bank energizing another recording was taken on the opposite capacitor bank 12.

Figure 1.29: Discrete Fourier Transform (DFT) plot of harmonic voltage content across relay element recorded whilst energizing capacitor 11.

Figure 1.30: Recorded voltage waveform during switching appearing across restricted earth fault relay on capacitor bank 12.
A Discrete Fourier Transform of the recorded voltage waveform in figure 1.30 indicates a high amount of harmonics in the secondary circuit.

Figure 1.31: Discrete Fourier Transform plot of harmonic voltage content across relay element recorded while energizing capacitor 12.

3.5.2 SCENARIO 2: DOUBLE BANK OUTRUSH SITE RECORDINGS

Recording of outrush currents was taken on the bank currently in service whilst energizing the other bank on the same set of busbars. The busbar voltage was not recorded in this scenario. The reason being the voltage source is extremely stable and showed no transient disturbances under single bank energizing. Furthermore the restricted earth fault relay is operated on current inputs from CT’s. It is these phase and neutral current that are required to induce voltages across the REF relay. However, one must appreciate the voltage signal of the source is required to determine the delay of the red phase breaker pole. It was however decided to use the delay from the first recording and apply it to simulations that follow. In addition it can be appreciated that the frequency of the outrush current is much higher than scenario 1. It is this higher frequency component which is responsible for added harmonic generation in the secondary circuit.
Figure 1.33: Recorded outrush current waveform taken during switching appearing across restricted earth fault relay on capacitor bank 11.

The voltage appearing across the REF relay during an outrush condition is shown figure 1.34. An increase in frequency is seen due to a decrease in source impedance. Furthermore this produces a higher magnitude of voltage across the relay terminals for the same time duration of the current transient shown above in figure 1.33.

Figure 1.34: Recorded REF voltage during capacitor bank 11 outrush.

Analysing these two recordings it is evident that there is a high harmonic component induced voltage appearing across the REF relay element during energizing conditions. Performing a DFT of the above voltage waveform using Omicron Enerlyser software displays a distinct pattern of voltages of higher harmonic order.
In order to validate the authenticity of the recordings, especially the phase and neutral currents used in the restricted earth fault circuit a software model was created. Under both condition no trip was on either capacitor bank. However high frequency harmonic voltages are recorded across the restricted earth fault relay.

### 3.5.3 Scenario 3: Double Bank Inrush Site Recordings

Unfortunately during the double bank inrush conditions recording of the voltage across the REF relay element was not possible. This is not a real concern as based on previous recordings it can be deduced that the profile of the voltage appearing across the REF element coincides closely with the inrush current transient profile. However the phase currents are recorded for inspection.
3.6 PROBABILITY OF SURGE ARRESTOR CONDUCTION DURING SWITCHING

It is reasonable to assume that surge arrestor conduction may be occurring during the breaker closing cycle. The only surge arrestors considered are the units that are encompassed by the REF protection circuit. As their conduction if sustained will cause the REF relay to trip. It would be difficult in practice to measure the transient voltage that would appear across the surge arrestor terminals. The reason being that there are no voltage instrument transformers located at that particular point in the bank making secondary measurement difficult. However one could analyze recorded data of surge arrestor conduction behaviour during transient conditions and establish similarities in current or voltage spikes. Similarly modelling their behaviour in a software platform will also provide useful insight.

3.7 PSCAD SIMULATION MODELS FOR SENARIO’S

3.7.1 INTRODUCTION

Software simulation provides a flexible platform for modelling the behaviour of power systems. It allows many different network scenarios to be configured and executed in very short amounts of time. Furthermore it allows the user to envisage the behaviour of electrical apparatus under different conditions. Size and location of electrical apparatus can easily be changed. However this is highly dependent on the accuracy of the data used to populate the model under scrutiny. It must also be appreciated that the designer may not have access to all the data that may be required for a 100% representation of the network. For these conditions the IEEE have compiled a report titled “Modelling Guidelines for Switching Transients”. The report provides a set of guidelines for conducting switching transient studies. This report was used as a guideline in the creation of the models used to investigate the system in question.

3.7.2 PSCAD MODEL PARAMETERS

In order for the model to reproduce realistic results it requires accurate data input. PSCAD allows the user to input the data though a graphic user interface liked to each network component. Data was sourced from the equivalent single line diagram of the network and used to populate the model. Due to their nature transients normally occur in very fast time intervals. In order to represent this in a simulation package a correct simulation time step is required. The smaller the time step chosen the more processing power is required and the longer it will take to provide a solution. The IEEE makes recommendations regarding the selection of the time step to be used during simulations. The time step shall be smaller than highest oscillatory frequency component. Other factors to consider are arrestor characteristics and minimum travel time of traveling wave line parameter models. A recommended time step in the range of 5 microseconds to 50 microseconds. In this case a time step of 5 microseconds was chosen. With this in mind the simulation will provide fairly accurate results as time step is significantly lower than highest resonant frequency of the capacitor bank.
3.7.2.1 Source Impedance Model

Results obtained earlier from the Digsilent model for the source impedances are reused in the PSCAD simulation model.

![Parameters used for network source model in simulation.](image)

Figure 1.38: Parameters used for network source model in simulation.

The three phase source model and general parameters for the source model in PSCAD are shown above. Due to the highly inductive nature of the network as shown by the high positive sequence impedance angle the source is modelled with primarily inductive impedance. In switching transient studies, the source is modelled as an ideal sine-wave source. Generators are modelled as a voltage behind a (sub-transient) Thevenin impedance. Often a network equivalent is used in order to simplify the representation of the portion of the power network not under study. [17] Furthermore the positive and zero sequence magnitudes are populated in this graphic user interface as well. These values are sourced from table 1-4.

![Positive and zero sequence source impedances required for accurate transient current flow calculations.](image)

Figure 1.39: Positive and zero sequence source impedances required for accurate transient current flow calculations.
3.7.2.2 Single Pole Breaker

The breaker or switchgear model includes three single pole circuit breaker control blocks. The switch or breaker is essentially modelled as an ideal conductor with zero impedance when in the closed position, and an open circuit of infinite impedance when the open state. PSCAD allows various options to vary the closing and opening time.

![Breaker modelled as three single breaker poles with zero resistance.](image1)

Furthermore the breakers are controlled by variable timers which are controllable via settable timers housed in the breaker Timed Breaker Logic GUI figure 1.41. The times can be manually adjusted affecting the closing times thus causing changes in transient response of model. The breaker pole closing times are measure form the original site recording and are shown below in table 1-8. These are used to populate the Timed Breaker Logic modules.

<table>
<thead>
<tr>
<th>Phase Breaker Pole</th>
<th>Red</th>
<th>White</th>
<th>Blue</th>
</tr>
</thead>
<tbody>
<tr>
<td>Close Time</td>
<td>2ms</td>
<td>6.946ms</td>
<td>3.480ms</td>
</tr>
</tbody>
</table>

Table 1-8: Closing Times used for poles derived from recordings

![Breaker closing times are set to the same times as measure from site recordings taking delays into consideration.](image2)

![Independent breaker pole control achieved by logic timers controlling closing times.](image3)

Breaker pre-striking is a common occurrence during capacitor bank energizing. Before the mechanical contacts of the breaker close an arc is established. The currents and voltages vary greatly and are dependent on the
characteristics of the breaker, network and point on voltage wave where closure occurs. This phenomenon is extremely difficult to predict and will not be considered in the model. However a normal transition is assumed for the closing of each breaker pole. If breaker pre-striking is considered, the distribution of closing angles is confined to the rising and peak portions of the voltage wave. A statistical switching method can be implemented in order to determine the suitability of a selected breaker but is beyond this scope of this study. Other consideration of breaker performance are temperature, SF6 pressure, hydraulic energy and dc voltage. [17]

### 3.7.2.3 Capacitor Bank Element

Each phase of the capacitor bank was simplified into an equivalent capacitance using applicable equations. However this excludes the red phase which was broken down into sub elements of capacitance. This was done to monitor the protection performance for faults close to the neutral point of the bank on individual cans. Faults close to the neutral point pose a problem due to low voltage levels and small fault current flow. Secondary parameters such as series inductance and loss resistance are not included in the model. The GUI for the capacitor element shown in figure 1.43 in PSCAD only provides a numerical input for the value of capacitance in uF.

![Figure 1.43: Input parameters for equivalent capacitance, this is applicable for both phase and earthing capacitance values.](image)

### 3.7.2.4 Current Transformers

This component is modelled in this specific PSCAD simulation using the Jiles-Atherton theory of ferromagnetic hysteresis. The effects of saturation, hysteresis remenance and minor loop formation are modelled based on the physics of the magnetic material obtained from the manufacturer of the current transformers. The current transformer measures a primary current as the input applies the algorithm and provides an output as the secondary current. In this simulation case the required data could not be obtained, the manufacturer of the current transformers insisted they could not divulge this information. Consequently a default value was selected on recommendation from PSCAD support services. However the following parameters for the current transformer could be populated realistically from values obtained from site.
3.7.2.5 Surge Arrester Model

The surge arrestors on the busbars are not considered whilst analysing the system response, only the arrestors protecting the reactor and surge capacitors on each phase is considered. The switching surge arrester model available in the Master Library is modelled as a piece-wise-linear resistance whose volt-amp characteristic is entered by the user (or a default characteristic can be applied). It is suitable for designing switching surge transient over voltage protection. Switch surge studies where not conducted on the model. The probability of surge arrester conduction was only considered. It can be noted that surge arrester conduction is most likely to occur during energization. This in turn gives rise to brief voltage transients within the bank and if above the rating of the surge arrester will be clamped to ground. Following on from the data collected on site, a zinc oxide ABB PLEXIM Q station class surge arrester was included protecting the inductors and earthing capacitors. The arrester characteristic is modelled by a number of exponential segments based on the arrester’s 30/60 microsecond current/voltage characteristics. These values are obtained from the arrester data sheet. Arrester current conduction and energy dissipation was monitored during capacitor breaker closing.
Figure 1.45: ABB Plexim surge arrestor Data Sheet.

The data sheet in figure 1.45, with the applicable surge arrestor characteristics for switching and lightning surges shown in blue indicates the surge arrestor conduction behavioural response when exposed to transient voltage waveforms. The values of the data sheet are used to populate the V-I characteristics of the surge arrestor in the model.

<table>
<thead>
<tr>
<th>Max. system voltage</th>
<th>Rated voltage</th>
<th>Max. continuous operating voltage</th>
<th>TOV capability</th>
<th>Max. residual voltage with current wave</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>as per IEC</td>
<td>as per ANSI/IEEE</td>
<td>MCOV 1 s</td>
<td>10 s</td>
</tr>
<tr>
<td>$U_{rms}$</td>
<td>$U_a$</td>
<td>$U_b$</td>
<td>$U_c$</td>
<td>$U_{peak}$</td>
</tr>
<tr>
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<td>108 kV</td>
<td>86 kV</td>
<td>86.0 kV</td>
<td>124 kV</td>
</tr>
<tr>
<td>120 kV</td>
<td>92 kV</td>
<td>66.0 kV</td>
<td>138 kV</td>
<td>132 kV</td>
</tr>
<tr>
<td>102 kV</td>
<td>92 kV</td>
<td>66.0 kV</td>
<td>158 kV</td>
<td>151 kV</td>
</tr>
<tr>
<td>144 kV</td>
<td>92 kV</td>
<td>115 kV</td>
<td>165 kV</td>
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</tr>
<tr>
<td>150 kV</td>
<td>92 kV</td>
<td>121 kV</td>
<td>172 kV</td>
<td>165 kV</td>
</tr>
<tr>
<td>162 kV</td>
<td>92 kV</td>
<td>131 kV</td>
<td>186 kV</td>
<td>178 kV</td>
</tr>
<tr>
<td>168 kV</td>
<td>92 kV</td>
<td>131 kV</td>
<td>193 kV</td>
<td>184 kV</td>
</tr>
</tbody>
</table>

Figure 1.46: Basic parameters of the surge arrestor used in the PASCAD model and specification of its I-V characteristic.

Figure 1.47: The 30/60 microsecond wave front characteristic is used to model the surge arrestor the data is used to populate the I-V characteristic table required in the model.
3.8 SCENARIO 1: SINGLE BANK INRUSH SIMULATION

A single bank simplified capacitor bank model was created in PSCAD ver 4.2. Controlled switching was implemented by staggering the circuit breaker closing times via delay blocks. This was done to try and replicate the point of wave synchronizing relay implemented on site. Delays are instituted in the control blocks based on closing times measured from site recordings. The aim was to prove the models transient response against the physical response of the system. For this reason if the results of the model and recordings are similar the model can be used for future capacitor bank installation transient studies.

Figure 1.48: Single capacitor bank energizing inrush current switching model constructed in PSCAD.
3.8.1 SIMULATION SINGLE BANK RECORDING

The phase currents for the above model were recorded for an energizing event and plotted in PSCAD.

Figure 1.49: Simulated phase current whilst energising a single 400kV shunt capacitor bank in PSCAD.

To emulate the voltage which would appear across the earth fault relay the three phase current transformer secondary currents are summated and subtracted from the neutral. This current is passed through an equivalent resistance to develop a voltage. The simulated voltage for single bank energizing which appears across the REF relay is shown in figure 1.50.

Figure 1.50: Simulated REF voltage whilst energising a single 400kV shunt capacitor bank in PSCAD.
3.9 SCENARIO 2: DOUBLE BANK OUTRUSH SIMULATION

The IEEE guide for switching transients tends to focus on the worst case switching scenario for transients i.e. double capacitor bank energizing. This is when the largest amounts of transient currents with higher than normal frequencies will flow in the system. The model used in the single bank scenario was simplified into an appropriate single line diagram model and simulated accordingly. This was also required as the PSCAD 4.2 version of software was a freeware version and limited node creation was available.

![Double capacitor bank energizing inrush current and outrush current model constructed in PSCAD.](image1.51)

3.9.1 SIMULATION DOUBLE BANK OUTRUSH RECORDING

The phase currents for the above model were recorded for an energizing and outrush event during energizing of a second capacitor bank and plotted in PSCAD. The result shown below in figure 1.52.

![Switching Simulation in PSCAD](image1.52)
The switching instances for each pole are set to be the same as the original recorded waveform.

As with the single bank inrush case the REF element voltage is measured in the same manner. This is achieved by summing the three phase current transformers and subtracting the neutral CT. The result is shown below in figure 1.53.

![Figure 1.53: Simulated REF voltage induced by outrush current when energizing an opposite 400kV shunt capacitor of equivalent size bank on local busbars in PSCAD.](image)

**3.9.2 SIMULATION DOUBLE BANK INRUSH RECORDING**

The phase currents for the above model were recorded for an energizing and outrush event during energizing of a second capacitor bank and plotted in PSCAD.

![Figure 1.54: Simulated REF voltage induced by outrush current when energizing an opposite 400kV shunt capacitor of equivalent.](image)

The simulation outrush and inrush waveforms are very similar in nature. The reason for this is discussed in chapter 4. The voltage across the REF element is not plotted as this was not initially recorded on site.
3.9.3 SURGE ARRESTOR CONDUCTION RECORDING DURING SWITCHING SIMULATION

The surge arrestors are required to protect the insulation integrity of the surge reactors and capacitors are used for inrush current suppression. If they are omitted from the circuit high voltages could develop across these devices and cause damage. Furthermore, these spikes normally of fair harmonic magnitude can be further impacting protection relay stability. One can see from the recorded waveform in PSCAD that the surge arrestors briefly conduct during the initial switching event. Their conduction is seen as short fast spikes.

The system simulation produced analogous results when compared to the recoded Comtrade files from site. It also indicated that the surge arrestors in the circuit briefly conduct when the point onto wave controller is going through its switching sequence. The simulated recordings also reiterated the presence of harmonics in the signal waveforms. At this stage in the analysis it is proven that there is a high harmonic voltage signal appearing across the REF relay input. This is the case during both switching events, but more so during double bank switching. The focus now shifts to the testing of the REF relay and investigated if any improvement can be made in the relays filtering capabilities.

Figure 1.55: Surge arrestor conduction during energizing of capacitor bank.
3.10 RESTRICTED EARTH FAULT RELAY TESTS AND REDESIGN

3.10.1 METHODOLOGY

In order to effectively test a device of any type there should be a comparable definition for the device describing how the device will perform. Usually this can be sourced from the product manual supplied by the manufacturer. The engineer conducting the test needs to be well acquainted with aspects relating to the functionality of the device under test.

In essence two facets of the protection relay are tested: selectivity and stability or security. Sensitivity will encompass the relays operating times when injected with voltage. Stability will include the behaviour of the relay whilst injected with non-ideal signals. The methodology adopted for testing the 7VH600 relay is based on a combination of both transient simulation and dynamic state testing. As it is suspected that the relay’s internal filtering circuitry operates inadequately for transient inputs rich in harmonics. Testing of the relay included injecting analogue signals rich in harmonics and checking the relays response. This included injecting the recorded energizing transient waveforms. Relay filtering tests and improvements to filtering circuitry are also conducted including monitoring the relays response to these modifications.

The statement obtained from the relay manual “The AC measured current is band pass filtered and rectified resulting in a dc voltage proportional to the input signal” is of particular interest. By definition a band pass filter is a filter that passes frequencies in a desired range and attenuates frequencies below and above that range. The tests for the relay input filtering characteristic is conducted with the settings on the relay fixed at 24V. The RMS value of the fundamental component is injected and relays operate time measured. The fundamental RMS voltage is increased and similarly the trip time is measured. Harmonic voltages from the 2\textsuperscript{nd} to the 9\textsuperscript{th} are superimposed on a fundamental voltage which is lower in magnitude as compared to the setting voltage. This harmonic voltage is injected into the relay and the response is monitored. Moreover the filtering circuit in the relay is monitored and a definite Fourier transform is performed for the input and output signals. If the filtering works the fundamental frequency should only propagate through the filter. For protective relays which rely on precise fundamental quantity’s post fault voltages and currents need to be extracted as quickly and as accurately as possible. An ideal filter is a narrow band pass filter [10]. Subsequently the relay is tested for its performance characteristics.
3.10.2 REF RELAY TEST 1 OPERATION TIME

The relays operational characterises where tested first. This included injecting voltages below and above the voltage setting and monitoring its trip output. It is found that for an increase in voltage above the nominal operation voltage of 26.5V the relays trip times decrease. This is clearly seen in figure 1.56.

![High Z Relay Trip Times](image)

Figure 1.56: Relay operate times for an increase in voltage above the setting voltage.

3.10.3 REF RELAY TEST 2 OPERATION TIME AND HARMONICS

Following on from the previous test the 7VH600 is injected with harmonic voltages from 50Hz up to 250Hz. The graph in figure 1.57 shows the relays operating time performance when injected with a ramping voltage signal at a fixed frequency. The frequenct ranged from 50Hz to 250Hz in 50Hz steps. It can be seen that the relays response is almost identical for all frequencies in the range. At this point it is established that the relay is not filtering out harmonic components in the input signal.

![Operation Time vs Voltage and Frequency Increase](image)

Figure 1.57: 7VH600 tripping time speed when injected with voltages with higher magnitudes and frequencies.
3.11 FILTER MODIFICATION

After Scrutinizing the schematic circuit diagram and PC board layout of the relay an intuitive decision is taken to install additional capacitive components to the filtering circuitry based on the succeeding context. It was decided that to improve the relays filtering ability a implementation of a low pass RC filter will be investigated. This approach was chosen with the aim to eliminate higher frequency components in the input circuit. Figure 1.58 is a basic schematic of a RC type filter. This is similar to the filter used in the REF relay.

![Series RC circuit](image)

**Figure 1.58: Typical RC filter topology.**

Essentially by increasing the value of capacitance in a low pass RC filter circuit the time constant $\tau$ is also increased. The existing time constant $\tau$ for the filter circuit is 121. However by the adding a 0.66uF capacitor in parallel $\tau$ changes to 781. By changing $\tau$ with the addition of capacitance the cut-off frequency is now reduced by 84.5%. Adding this capacitance will aid the circuit at low frequencies as it has time to charge, and so the voltage across the capacitor is almost equal to the input voltage. However at high frequencies, the capacitor is only able to charge up to a smaller value before the input changes direction due to its sinusoidal nature. When the zero crossing transition occurs in the sine wave the capacitor begins to discharge. With this in mind it can be appreciated that the output voltage will decrease fractionally when compared to the output of the original capacitance value. The higher the frequency, the slower the output response is due to the time delay attributed to the capacitor. The output is attenuated at a frequency above the cut-off frequency.
Therefore, since only a small fraction of the input is able to flow through as driving voltage, the remainder of the input flows through the capacitor to ground. Adding a higher capacitance will decrease the filter circuit’s impedance at higher frequencies. Therefore allowing higher frequency components to be shunted away from entering the threshold trigger portion of the circuit. The capacitance in red is added to the circuit as shown below in figure 1.59. With the value of capacitance chosen the next step was to test the response of the filter with it’s modified input filtering capabilities.

Figure 1.59: Basic test principle used for testing REF relay filtering. Indicates where capacitors are added to improve filtering circuitry.
3.11.1 REF RELAY TEST 3 STANDARD FILTER

The relay is tested at a nominal setting voltage of 24V at fundamental frequency and ramped voltage in 100mV steps at a rate of 1 second. Relay operation occurred at 26.5 V relay and tripped in 49ms this is with no additional filter modifications. The pre bridge rectifier voltage remained at 3.48V and post bridge rectifier voltage was 2.41V.

![Figure 1.60: Standard filter response to setting voltage.](image)

3.11.2 REF RELAY TEST 4 MODIFIED FILTER

Tested relay at nominal setting voltage of 24V at fundamental frequency and ramped voltage in 100mV steps at a rate of 1 second. Relay operation occurred at 26.5 V and tripped in 30.96ms this is with the addition of a 0.66µF capacitor to the filter circuit. The pre bridge rectifier voltage remained at 3.41V and post bridge rectifier voltage was reduced 2.38V.

![Figure 1.61: Modified filter response to setting voltage.](image)
3.11.3 REF RELAY TEST 3 VOLTAGE SPIKE NORMAL FILTER

During this test a recorded voltage waveform was injected, the recording was one of the recordings taken whilst energizing. The recording was increased to 7.4 pu as the original recording did not cause the relay to trip when injected. The relay trip occurred in 21.653ms. Pre rectifier voltage was measured to be 1.64V and post rectifier voltage measured 1.15V respectively. Furthermore, the waveform had a R.M.S value of 13.1V and a contained a fundamental 50Hz component of 9.99V.

Figure 1.62: Injected transient recorded waveform and relay response to standard filter.

3.11.4 REF RELAY TEST 4 VOLTAGE SPIKE MODIFIED FILTER

A 0.66uF capacitor was added to the filter circuit. The same recorded voltage waveform as above was injected and the following results obtained. Pre rectifier voltage was measured to be 0.94V and post rectifier voltage measured 0.44V respectively. As before the waveform had a R.M.S value of 13.1V and a contained a fundamental 50hz component of 9.99V.

Figure 1.63: Injected transient recorded waveform and relay response to modified filter.
3.11.5 REF RELAY TEST 5 VOLTAGE 20% 2nd HARMONIC NORMAL FILTER

This test consisted of injection of a second harmonic voltage of 20% superimposed on fundamental voltage setting. This test was performed with a range of harmonic ranging from the 2nd to the 9th all 20% in magnitude. The results for the 2nd harmonic tests are shown below in figure 1.64.

![Figure 1.64: Injection of 20% 2nd harmonic superimposed on fundamental into standard filter.](image)

3.11.6 REF RELAY TEST 6 VOLTAGE 20% 2nd HARMONIC MODIFIED FILTER

The second harmonic injection with the addition of the Capacitor, caused the tripping time of the relay to be delayed by half a cycle 10ms. An inherent phase shift can be seen due to addition of capacitance to the circuit.

![Figure 1.65: Injection of 20% 2nd harmonic superimposed on fundamental into modified filter.](image)
3.12 FINDINGS

The capacitor bank inrush calculations provide theoretical values for the worst case expected inrush current that can be experienced. These calculations can then be used to provide a guide when calculating the setting voltage for the REF relay. Other considerations such as CT characteristics and secondary circuit impedances also need to be considered and will affect the setting voltage and relay operation. Furthermore a software system simulation can be used to verify transient inrush currents that will be present upon capacitor bank energizing. Software simulation results are heavily dependent on accurate model input parameters in order to provide correct results. In cases where parameters are unavailable realistic assumptions need to be made based on previous case studies or standards. The best way to validate a systems response is to view the systems behaviour real-time or conduct a recording. This allows for in-depth analysis of the systems actual response in the network. Similarly the recording can then be used to cross reference the simulation model and authenticate its characteristics. Although software simulations provide fast result and save resources, they still cannot outweigh tangible site data recordings.

The presence of unsymmetrical harmonic transients in the inrush and outrush current recordings indicates that there is a probability of incorrect relay operation if the relays filter design is inadequate. Based on this realization the relays operation and filtering are investigated. The relay was tested at its present voltage setting with various harmonic signals and found to be susceptible to harmonics. It was then decided to test and analyse the relay filtering circuitry. At this stage it was discovered that the relay filtering was insufficient. It was decided to improve the filter circuit by increasing the capacitance of the low pass filter therefore increasing the time constant tau of the circuit. By doing this the cut off frequency is also reduced. The modified relay filter circuit performance was found.
4.1 INTRODUCTION

Data analysis by definition is a body of methods that help to describe facts, detect patterns, develop explanations, and test hypotheses. This chapter strives to evaluate and comment on the relevant calculations, recordings and simulations conducted to investigate the problem at hand. The aim is to discover a common trend in the data which can be used and applied to problems of a similar nature. As previously stated two capacitor bank energizing scenarios are recorded being single and double bank energizing. Furthermore the relays filtering capabilities are tested.

4.2 DATA COLLECTION AND ANALYSIS

The data collection process consisted of sourcing and processing of all relevant site recordings for the two different switching scenarios. Similarly signal processing capability recordings from the relay including filter testing results and operational characteristics are presented and discussed.

4.3 CAPACITOR BANK INRUSH AND SETTING CALCULATIONS

By using the IEEE Std 1036-2010 for calculation of capacitor bank inrush currents the setting engineer can establish the most plausible worst case inrush current condition. The IEEE standard chooses to exclude the effect of the series resistance in the circuit.

Furthermore for single and double bank energizing the magnitudes of inrush current calculated are only applicable at a voltage rating of 1 p.u. If the voltage increases the inrush current increases and vice versa. This should be considered when choosing an appropriate setting as voltage conditions on the busbars are vary according to network loading. Therefore it would be advisable to reduce the system voltage before energizing the capacitor banks thus limiting the magnitude of inrush current experienced.

Essentially when selecting the voltage setting one needs to consider the effects of choosing the setting value on the REF relay of 48V opposed to 120V. Similarly the selection of these values will have a direct effect on the protection security and sensitivity. A setting selection of 48V will yield the most protection coverage of the capacitor bank detecting faults closer to the neutral, whilst the 120V setting will prove to be the most stable under worst inrush conditions but at the cost less earth fault bank coverage. Furthermore the use of a point on wave switching controller and inrush current limiting reactors will aid in limit the inrush current further.
4.4 RECORDINGS AND SIMULATIONS

The PSCAD software model aided in visualising the behavioural response of the system when energizing a single bank as opposed to double bank energizing conditions. Additional models are also created to simulate earth fault conditions in the bank. The values of these simulations for both energizing and fault conditions where compared to calculated values and proved to be rationally accurate.

The peak values of phase currents from both recorded and simulated results are shown below in table 1-9. The three different cases are considered and compared for authenticity. The breaker poles are switched according to the times shown in table 1-8. These times are obtained from the initial recording shown in figure 1.27. The results produced an acceptable result for double bank energizing conditions. However the single bank model deviated substantially on the red and white phase currents. This is related to the sharp spikes seen on the recording in figure 1.11 caused by the non-linear nature of surge arrestor conduction.

<table>
<thead>
<tr>
<th>Comparison of Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantities in secondary values from CT outputs</td>
</tr>
<tr>
<td>Phase</td>
</tr>
<tr>
<td>Single Bank Inrush Peak</td>
</tr>
<tr>
<td>Single Bank Outrush Peak</td>
</tr>
<tr>
<td>Double Bank Inrush Peak</td>
</tr>
</tbody>
</table>

Table 1-9: Inrush current peaks in secondary circuit of recorded values vs simulation values.

It must be noted that the recorded source voltages is only of particular importance when it comes to the energizing of the capacitor bank. The higher the p.u value of the source voltage the greater the magnitude of inrush current will be experienced. Consequently this will affect the voltage appearing across the restricted earth fault relay circuit input. Furthermore harmonics in the source voltage will also affect the stability of the protection circuit. The recorded source voltage was analysed via a Discrete Fourier Transform and found to contain very low percentages of harmonics. Therefore it is assumed to be purely a 50Hz source voltage.
4.5 SINGLE BANK INRUSH

A harmonic analysis on the REF circuit voltage appearing across the relay of capacitor bank 11 is shown in chart 1-2. It can be seen that the predominant harmonics occur in the lower harmonic frequency ranges. This can be expected due to the interaction between the source impedance and the impedance of the capacitor bank.

Chart 1-2: Harmonic content of recorded voltage across restricted earth fault relay element for single bank in rush capacitor bank 11.
In addition an harmonic analysis is performed on the voltage recording taken across REF element of capacitor bank 12. The Discrete Fourier Transform of the voltage waveform reveals that this particular transient contained even more harmonics than the previous case of capacitor bank 11. This can be expected due to the transient behaviour of the circuit during energizing conditions and the high frequency oscillations between the two banks.

Chart 1-3: Harmonic content of recorded voltage across restricted earth fault relay element for single bank inrush capacitor bank 12.

The DFT analysis results for software simulation are shown in chart 1-3. This is the percentage of harmonic found in the simulated recorded waveform and reveals a similar harmonic content when compared with the energizing recording of capacitor bank 11 shown in chart 1-2. The causes for the differences can be attributed to the non-linear nature of the circuit. Moreover the model used in the simulation does not include stray inductances and capacitance in the circuit. Similarly the busbar inductance and mutual coupling of the two capacitor banks is assumed to be ideal. Another factor to consider is the percentage errors in the recording equipment.
Chart 1-4: Simulated harmonic content of voltage appearing across restricted earth fault relay for single bank energizing condition.
4.6 DOUBLE BANK INRUSH AND OUTRUSH SITE RECORDINGS

The voltage appearing across the REF relay during double bank inrush conditions were not recorded and analysed. However the currents are recorded and are very similar when compared to the outrush recording of capacitor bank 11. To prove this the two recorded scenarios are superimposed on one another and a DFT analysis is performed on the red phase current for both conditions and harmonic contents compared.

Figure 1.66: Recorded inrush current during energizing of capacitor bank 12 with capacitor bank 11 in service.

The comparison of the harmonic contents of the red phase phase currents during outrush vs inrush is shown below in chart 1-4. It is evident that the relationship between inrush and outrush harmonic content on the capacitor bank is similar in nature. The largest difference appears in the higher harmonic orders and is a result of the higher magnitudes of harmonic currents experienced during inrush and outrush conditions.

Chart 1-5 Harmonic analysis of percentage difference for recorded current waveforms for outrush and inrush conditions.
An harmonic analysis of the voltage across the REF relay during outrush transient conditions for capacitor bank 11 is shown in chart 1-6. It can be seen that the predominant harmonics occur in the higher harmonic frequency ranges. This can be expected as there is a reduced impedance between the two capacitor banks. The impedance is 18.7 times smaller than the source impedance and is responsible for higher inrush currents.

Chart 1-6: Harmonic analysis of recorded REF voltage waveform for outrush of capacitor bank 11 energizing capacitor bank 12.

As with the single bank energizing simulation the busbars inductance is neglected as well as mutual coupling. This effectively reduces the total inductance of the circuit and will give rise to a higher harmonic content in the energizing currents. This creates a voltage waveform across the REF relay which is richer in harmonics when compared to the recoded waveform.

Chart 1-7: Simulated voltage appearing across restricted earth fault relay during outrush
4.7 RELAY TESTING AND FILTER CIRCUIT HARMONIC REDUCTION

Testing of the high impedance earth fault relay provided useful insight into possible cases of maloperation of the relay when exposed to harmonic content. In essence when the relay was injected with voltage signals containing harmonics greater than the fundamental at the setting voltage it operated. However when the relays filtering circuitry was improved it proved to be stable when injected with harmonics at its setting voltage.

Although there are multiple tests performed on the relay and its filtering circuitry the test of particular interest is the response of the relay when injected with the voltage spike recorded during single bank energizing conditions shown in figure 1.27. The way relay responds to this dynamic waveform will give insight into its response to harmonic voltage waveforms. Testing the 7VH600 by injecting the recorded voltage from the single bank energizing condition was increased by a factor of 7.4 pu. The relay trips for this condition at 13.498 Vrms peak. This was the behaviour of the relay voltages without the addition of the capacitor into the filtering circuitry. The Relay tripped in 21.94ms.

Figure 1.67: R.M.S representation of voltage across standard filter circuit during single bank energizing conditions.
A table illustrating the percentage harmonic content found in the filter circuit when injected with the waveform is shown below in Chart 1-8.

<table>
<thead>
<tr>
<th>Harmonic</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.00%</td>
</tr>
<tr>
<td>3</td>
<td>50.00%</td>
</tr>
<tr>
<td>5</td>
<td>100.00%</td>
</tr>
<tr>
<td>7</td>
<td>150.00%</td>
</tr>
<tr>
<td>9</td>
<td>200.00%</td>
</tr>
<tr>
<td>11</td>
<td>250.00%</td>
</tr>
<tr>
<td>13</td>
<td>1.00%</td>
</tr>
<tr>
<td>15</td>
<td>1.00%</td>
</tr>
<tr>
<td>17</td>
<td>1.00%</td>
</tr>
<tr>
<td>19</td>
<td>1.00%</td>
</tr>
<tr>
<td>21</td>
<td>1.00%</td>
</tr>
<tr>
<td>23</td>
<td>1.00%</td>
</tr>
<tr>
<td>25</td>
<td>1.00%</td>
</tr>
<tr>
<td>27</td>
<td>1.00%</td>
</tr>
<tr>
<td>29</td>
<td>1.00%</td>
</tr>
<tr>
<td>31</td>
<td>1.00%</td>
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<td>33</td>
<td>1.00%</td>
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</tr>
<tr>
<td>57</td>
<td>1.00%</td>
</tr>
<tr>
<td>59</td>
<td>1.00%</td>
</tr>
</tbody>
</table>

Chart 1-8: Percentage of harmonics in standard filter circuit when injected with energizing transient waveform.

With the addition of the Capacitor into the filtering circuit the relay responds to the same fault differently by not tripping. Similarly there is a reduction in the propagation of harmonic voltage to the Schmitt trigger. This can be attributed to the harmonic filtering characteristic the capacitor provides to the unfiltered signal. This is clearly seen by a reduction in magnitude and phase shift of the filter input and output signals.

Figure 1.68: R.M.S representation of voltage across modified filter circuit during single bank energizing condition with modified filter showing reduction in voltage.
A chart illustrating the percentage harmonic content found in the filter circuit when injected with the waveform is shown below in chart 1-9.

![Harmonic content of transient through filter](chart.png)

Chart 1-9: Percentage of harmonics in standard filter circuit when injected with energizing transient waveform

It was found that the relay operated at a substantially lower voltage for higher frequencies than those of the setting voltage at 50Hz. The relay is injected with a 20% harmonic content of the nominal setting voltage up to the 9\textsuperscript{th} harmonic. Relay operate times for injected voltages are shown below in table 1-10.

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Pre Rectifier Volts</th>
<th>Post Rectifier Volts</th>
<th>Trip Time ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd</td>
<td>3.54</td>
<td>2.51</td>
<td>18.2</td>
</tr>
<tr>
<td>3rd</td>
<td>3.9</td>
<td>2.79</td>
<td>25</td>
</tr>
<tr>
<td>4th</td>
<td>3.81</td>
<td>2.79</td>
<td>19.2</td>
</tr>
<tr>
<td>5th</td>
<td>3.84</td>
<td>2.78</td>
<td>18.2</td>
</tr>
<tr>
<td>6th</td>
<td>3.82</td>
<td>2.79</td>
<td>17.6</td>
</tr>
<tr>
<td>7th</td>
<td>3.82</td>
<td>2.78</td>
<td>17.2</td>
</tr>
<tr>
<td>8th</td>
<td>3.81</td>
<td>2.78</td>
<td>17.1</td>
</tr>
<tr>
<td>9\textsuperscript{th}</td>
<td>3.81</td>
<td>2.79</td>
<td>18.1</td>
</tr>
</tbody>
</table>

Table 1-10: Standard relay circuitry response when a nominal setting voltage is injected with 20% harmonic content superimposed on fundamental.
Moreover the voltages across the filter and output of the rectifier to the Schmitt trigger circuit are measured for the different harmonic voltages. The results and operation times are shown below in table 1-11.

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>With Addition of 0.66uf Capacitor to Pre Rectifier Volts</th>
<th>Post Rectifier Volts</th>
<th>Trip Time in ms</th>
<th>% Rms output reduction to Schmitt Trigger</th>
<th>% Time Increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd</td>
<td>3.31</td>
<td>2.32</td>
<td>31.3</td>
<td>7.569721116</td>
<td>41.85303514</td>
</tr>
<tr>
<td>3rd</td>
<td>3.55</td>
<td>2.47</td>
<td>54.1</td>
<td>11.46953405</td>
<td>47.55859375</td>
</tr>
<tr>
<td>4th</td>
<td>3.44</td>
<td>2.44</td>
<td>20.3</td>
<td>12.54480287</td>
<td>5.418719212</td>
</tr>
<tr>
<td>5th</td>
<td>3.45</td>
<td>2.43</td>
<td>19.3</td>
<td>12.589931200</td>
<td>5.699481865</td>
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<tr>
<td>6th</td>
<td>3.42</td>
<td>2.4</td>
<td>30.2</td>
<td>13.97849462</td>
<td>41.72158543</td>
</tr>
<tr>
<td>7th</td>
<td>3.43</td>
<td>2.41</td>
<td>27.7</td>
<td>13.30935225</td>
<td>37.90613718</td>
</tr>
<tr>
<td>8th</td>
<td>3.39</td>
<td>2.38</td>
<td>29.2</td>
<td>14.3884921</td>
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</tr>
<tr>
<td>9th</td>
<td>3.38</td>
<td>2.38</td>
<td>29.6</td>
<td>14.693405</td>
<td>38.85135135</td>
</tr>
</tbody>
</table>

Table 1-11: Modified relay circuitry response when a nominal setting voltage is injected with 20% harmonic content superimposed on fundamental.

4.8 FINDINGS

In conclusion the difference in simulation and recorded values can be attributed to the lack of data and element parameters used in the software model. This includes busbar inductances, current transformer core dimensions and the fact that dynamic source impedance is constantly changing, as well coupling capacitances of the apparatus. However the behaviour of the model is still practicable when compared to the site recordings. It should be appreciated that both the model and recordings indicate a high amount of harmonics during the switching transient events. It is there transient inrush harmonics that are causing the relay to trip. The phenomenon of outrush currents on capacitor banks is not exclusive to back to back capacitor bank energizing scenario’s. Outrush currents of various proportions and harmonic frequencies will also occur for faults on other system apparatus. It is these harmonics propagate through the secondary circuit and appear across the REF element as a voltage. The energizing transient harmonics are responsible for jeopardizing the security of REF relay. The inability of the present REF relay filter to remove these harmonics from the signal causes it to operate. It is found that by a minor inexpensive modification the filter circuit can be substantially improved thus filtering out harmonics found during inrush transient conditions. The filter modification alters the relay operating times to some degree but operational times still fall within permissible limits. The relays operating times is heavily dependent on the voltage level applied. The greater the voltage level compare to the setting threshold the faster the relays operating time will be. Moreover tripping times will also vary based on the type of harmonics present in the system and where on average 10ms slower.
5.1 CONCLUSIONS

The conclusion may be drawn from the findings that the initial calculations by the utility settings engineer for the restricted earth fault relay settings are questionable. It was found that the setting engineer used the incorrect magnetization currents obtained from the current magnetization curves in the initial setting calculations. This together with the assumption of the magnitude of inrush current led to the selection of a setting of 24V which was shown as being too sensitive. With the 24V setting on the restricted earth fault relay and poor transient filtering of the relay spurious tripping can be expected due to high harmonic content as shown by the inrush and outrush current recordings. Assuming an energizing inrush current of ten times the nominal rated current may work in some cases but it is not a true reflection when compared to calculated values of Inrush current. Is it more reliable to use the IEEE standard for energizing inrush calculations as their results yield the worst possible inrush current magnitude capability of the required breaker. However, their calculations are based on using a DC source in a LC switching circuit and do not consider all effects of the power system. The benefit of using this calculation method is that it provides a fast analytical result. If the setting engineer wishes to achieve a higher level of accuracy in determining the peak inrush current a more advanced calculation may be performed. This can include the use of differential equations etc. The probability on the inrush current reaching such a level is highly unlikely as there is normally damping circuitry added to the capacitor bank to aid in reducing its magnitude.

The conclusion may be drawn that the point on wave switching controller is proven to reduce inrush current magnitudes when switching falls within permissible set time limits. However these time limits are influenced by external factors which are uncontrolled such as temperature, breaker operating time drift and mechanical behaviour. A 1ms delay in closing of a breaker pole on the voltage waveform is enough to produce a substantial phase transient current of high harmonics. This is even worse in the case of back to back energizing. This in turn creates a spill current in the REF relay circuit due to the imbalance of phases in the circuit. If closing is delayed long enough the effective harmonic transient current may be enough to cause relay operation. The mechanical operation of the breaker is difficult to predict its operational time with precise accuracy, there by resulting in closing on different points on the voltage wave thus producing varying amounts of transient harmonic inrush currents.

It must be understood that REF protection is not classically applied to SCB’s so its characteristics and requirements should be carefully considered and understood when it is implemented in other scenarios. This means the associated transient phenomenon’s of the particular equipment must be fully analysed to prevent spurious tripping during these events. When energizing a single isolated capacitor bank from a predominantly inductive source. It can be noted that a high-frequency, high-magnitude current flows into the capacitor bank this can attributed to the fact that the bank is trying to equalize the system voltage and the capacitor voltage [7]. These inrush currents may cause CT saturation if they are of a substantially large magnitude. Careful
consideration should also be made when selecting protection relays. As inadequate filtering of harmonics will affect the protection circuit’s performance. Older type static relays using exclusively low pass filters may prove to be troublesome as their performance may diminish with high harmonic currents. Controlled switching may pose a potential problem for protection circuits especially in REF if closing time delays are exceeded and switching takes place on higher points of the voltage wave.

It is possible that surge arrestor conduction may be occurring during switching as transient voltages propagate through the bank as shown by the simulation result in figure 1.66. The conclusion may be drawn that this is not the real cause of the REF relay operation, as the duration of these conduction spikes are very fast (in the order of 3ms). Therefore, due to the operation time of the REF relay falling between 20ms and 40ms proves stability during these short conduction periods. In addition the effects of current spikes produced by conduction on the relay can be further reduced by improved relay filtering.

As seen in the setting calculations the inrush current in eq (18) and eq (20) will play a pivotal role in the selection of the voltage setting. If the busbar voltage exceeds the nominal 1 p.u. which is often the case during lightly loaded periods the value the inrush current will increase if the bank is energized. The conclusion may be drawn that it is reasonable to sacrifice sensitivity in terms of protection settings for increased security. This however is dependent on the nature of the plant being protected. Protection systems are required to be secure and reliable. Furthermore it is clear from testing the relay that its filtering capabilities are questionable and unreliable. The conclusion may be drawn that reliability of the relay can be improved with the addition of improved filtering circuitry. However, this alters the relays response time during fault conditions. Nevertheless, the addition of circuitry to the relay input filter still provided acceptable operation times. In some cases the tripping times where faster.

5.2 RECOMMENDATIONS

The use of IEEE standards when calculating capacitor bank inrush setting calculations should be strongly considered when performing transient inrush setting calculations. Furthermore it can be clearly seen that the magnitude of inrush current seen in the fault recording does not accurately correlate to the assumption made for inrush current on the setting sheet, the original assumption was 10 times the nominal current resulting in a 24V REF relay setting. Consequently selecting this low setting this will directly affect the stability of the protection circuit. In this specific case the setting needs to be increased to 48V for single bank energizing and a sufficient value for double bank energizing conditions is calculated to be 96V. However the setting of 48V will most probably prove to be stable for double bank energizing conditions as the point on wave switching controller and inrush reactors will limit the inrush current. Furthermore the 48V setting will provide better fault coverage closer to the neutral of the bank as compared to the 96V setting. The improved filter circuit will also assist in this regard and make the relay more secure under double bank energizing conditions.

An enhanced solution would be to replace the relay with a modern numerical high impedance REF relay. Modern numerical relays allow protection engineers to implement advanced protection logic at a attractive cost.
Furthermore they have digital filters and can filter out the large amounts of high frequency inrush currents associated with SCB energizing. The relay will normally contain all the required protection elements within one device allowing for advanced logical protection control functions to be used. The selection of a restricted earth fault relay with adequate filtering capabilities will greatly enhance the security of the restricted earth fault circuit. This is easily achieved by replacing the relay on site with a modern numerical relay. The only requirement would be to calculate new setting parameters for the modern relay. Modern numerical relays use anti-aliasing type filters which are less susceptible to transient waveforms. They can effectively derive the fundamental frequency required for a calculated setting threshold comparison.

An added benefit of opting for the installation of a modern numerical relay includes the on board fault recording capabilities present within the majority of these newer numerical relays. In the event of a fault the relay can be configured to trigger an oscillography record capture and will store the data locally on the device. This can be taken one step further by connecting the relay through an applicable communications medium to a GSM modem allowing a user to interrogate the relay remotely retrieving records and altering settings if required.

An alternative practical approach would be to introduce a delay in the protection relay operation circuitry. The delay can be initiated by a close command from the breaker and readable the real after the last breaker pole closure. This will block the restricted earth fault protection form operating whilst the breaker goes through its closing cycle. The only disadvantage of this approach is it does not take care of outrush current conditions on opposing banks which occur during double bank energizing conditions. In addition, while the REF relay is disabled there is a risk involved of sustaining plant damage due to possible faults occurring in this period and not being detected and cleared.
CHAPTER 6 - LIST OF REFERENCES


APPENDIX

SYMBOLIC DEFINITIONS

\( i = \) nominal phase current
\( I_{pse} = \) r.m.s value of primary symmetrical short circuit current
\( T_p = \) primary time constant
\( \phi = \) angle of switching on volge wave
\( \alpha = \) phase angle difference between voltage and current
\( f = \) nominal system frequency in Hz
\( R = \) resistance in Ohm’s
\( X_C = \) capacitive reactance in Ohm’s
\( X_{CE} = \) earthing capacitive reactance Ohm’s
\( C = \) capacitance in Farads
\( X_L = \) inductive reactance in Ohm’s
\( X_{ls} = \) inductive reactance of source in Ohm’s
\( L = \) inductance in Henry
\( Z = \) impedance in Ohm’s
\( Z_{cer} = \) equivalent earthing capacitor impedance in Ohm’s
\( Z_t = \) total capacitor bank impedance in Ohm’s
\( C_{eq} = \) equivalent phase capacitance in Farads
\( I_{full\ load} = \) full load current of the capacitor bank in Amperes
\( V_{LS} = \) voltage across the source inductance in Volts
\( V_{RS} = \) voltage across the source resistance in Volts
\( I_{cb} = \) current flowing through capacitor in Amperes
\( \zeta = \) damping factor
\( \omega_n t = \) natural frequency
\( \theta_n = \) angle of resonant frequency
\( C_{b1} = \) total capacitance of capacitor bank 11
\( C_{b2} = \) total capacitance of capacitor bank 12
Fc = frequency of inrush current for single bank
F_{c1,c2} = frequency of inrush current for double bank
V_{eff} = effective setting voltage of REF relay
R_{CT} = winding resistance of secondary CT circuit
R_{LEAD} = lead resistance of secondary cables
n = place on string where fault occurs
S = number of elements in string
LIST OF EQUATIONS

\[ i = \sqrt{2} \times I_{psc} \left[ e^{\frac{j\phi}{\sqrt{2}}} \cos(\phi - \alpha) - (\cos \omega t + \phi - \alpha) \right] \] (Eq 1)

\[ Xc = \frac{1}{2\pi f \times c} \] (Eq 2)

\[ Xce = -j \frac{1}{2\pi f \times c} \] (Eq 3)

\[ Zcer = \frac{Xc \times R}{Xc + R} \] (Eq 4)

\[ X_L = 2 \times \pi \times f \times L \] (Eq 5)

\[ Zt = -jX_{\text{phase}} + Z_{\text{cer}} + jX_L \] (Eq 6)

\[ C_{eq} = \frac{1}{2\pi f \times x_t} \] (Eq 7)

\[ I_{\text{full load}} = \frac{V_{\text{line}}}{\sqrt{3}} \times \frac{1}{x_t} \] (Eq 8)

\[ L_s = \frac{x_s}{2\pi f} \] (Eq 9)

\[ V_s = V_{LS} + V_{Cb} + V_{Rs} \] (Eq 10)

\[ V_{LS} = L_s \frac{di}{dt} \] (Eq 11)

\[ i_{Cb} = \frac{1}{C} \int i \ dt \] (Eq 12)

\[ V_{Rs} = R_s \] (Eq 13)

\[ V_s \sin (\omega t + \phi) = \frac{d^2i}{dt^2} + \frac{1}{Lc} i + \frac{R}{L} \frac{di}{dt} + Vc(0) \] (Eq 14)

\[ \zeta = \frac{a}{\omega} \] (Eq 15)

\[ \omega = \frac{1}{\sqrt{Lc}} \] (Eq 16)

\[ f_c = \frac{\omega}{2\pi} \] (Eq 17)
\[ I_{\text{peak max}} = 1000 \times V_{LL} \sqrt{\frac{2}{3}} \times \sqrt{\frac{C_{eq}}{L_{eq}}} \]  
(Eq 18)

\[ C_{eq} = \frac{C_{b1} \times C_{b2}}{C_{b1} + C_{b2}} \]  
(Eq 19)

\[ I_{\text{peak max}} = 1000 \times V_{LL} \sqrt{\frac{2}{3}} \times \sqrt{\frac{C_{eq}}{L_{eq}}} \]  
(Eq 20)

\[ V_{\text{eff}} > \frac{I_{\text{inrush}}}{C_{T\text{ratio}}} \times (R_{CT} + 2 \times R_{\text{LEAD}}) \]  
(Eq 21)

\[ I_{ct \text{ phase}} = V_{\text{eff}} \times \left( \frac{I_{\text{knee phase ct}}}{V_{\text{knee phase ct}}} \right) \]  
(Eq 22)

\[ V_{\text{varistor}} = K \times I^{B} \]  
(Eq 23)

\[ I_{\text{eff}} = [3 \times I_{ct \text{ phases}} + I_{ct \text{ neutrat}} + I_{\text{relay}} + I_{\text{var}}] \times C_{T\text{ ratio}} \]  
(Eq 24)

\[ C \text{ (faulted string)} = \frac{n}{5-n} \]  
(Eq 25)
OMICRON CMC356 CALIBRATION CERTIFICATE

Certificate of Calibration and Conformance

Conformance
OMICRON electronics GmbH certifies that the product detailed below (Device Type, Serial No) has been designed, manufactured, tested, adjusted and calibrated to the highest quality standards of workmanship and materials in compliance with a quality system registered to ISO 9001:2000 (SGS Austria Control-GmbH, certificate number AT009045).

The product conforms to all specifications published in the manual and has passed all tests successfully.

More detailed test data can be found on the enclosed CD/DVD in the directory Report. Warranty (one year) and calibration are valid from Date of Issue.

Traceability Information
Traceability is to national standards administered by EURAMET and ILAC members (e.g. OKD, DKD, NIST, NATa, NPL, PTB, BMU etc.) or other recognized standard laboratories. Some measurements are traceable to natural physical constants, consensus standards or ratio type measurements.

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SNo: DF038F
Option: NET-1, ELT-1
Calibration Date: 2010-08-20

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Date of Issue: 2010-08-27

Manager Operations: Dietmar Gehrmann
Testengineer: Markus Märk
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Restricted Earth Fault relay application on Shunt Capacitor Bank Design with Synchronized Switching

W. Minkley
Eskom – Power and Energy Utility
East London, South Africa
minkwa@eskom.co.za
East London, South Africa

W. Phipps, R. T Harris, AG Roberts
NMMU – Nelson Mandela Metropolitan University
Port Elizabeth, South Africa
william.phipps@nmmu.ac.za, raymond.harris@nmmu.ac.za
alan.roberts@nmmu.ac.za

Abstract—This paper is aimed at analyzing the performance of restricted earth fault relay protection used in conjunction with controlled switching on a 400kV 100 MVAR capacitor bank scheme used on the Eskom Transmission network. After the commissioning of the capacitor bank using the above mentioned scheme design the plant was energized. The capacitor bank then experienced spurious trips. The cause of the trips was the operation of the restricted earth fault relay.

In this investigation, restricted earth fault protection on Shunt Capacitor Banks in the Eskom Transmission environment will be the area of interest. The research will analyze the current Shunt Capacitor Bank protection scheme in service specifically looking at the restricted earth fault circuit design and relay performance. An equivalent model of the Shunt Capacitor Bank from primary plant perspective based on theory is derived. Recording and analyzing of Comtrade transient waveforms respectively, when the bank is energized, will be done in order to provide a reference to work from. Manual calculations of various parameters from the derived model including harmonics, transients, inrush currents and fault currents will be performed to access scheme parameters.

Index Terms— shunt capacitor bank, restricted earth fault protection, electromagnetic transient simulation, capacitor energizing transient, controlled switching

I. INTRODUCTION

Each phase of the shunt capacitor bank is constructed in two stacks or banks interconnected by cables with capacitively earthed neutrals so that a conventional voltage differential protection scheme can be used. The bank is of the fuseless construction which is preferred by Eskom because this technology has proven to be reliable and easy to maintain [1]. Fuseless capacitor banks mainly utilize an unbalance protection scheme as the primary means of protection. As the name implies, there are no internal or external fuses on this design. Their "string" configuration provides a very reliable and cost effective design for banks rated at 35 kV and above [2].

During the final commissioning phase when one of the Shunt Capacitor banks (SCB) was energised the Restricted Earth Fault (REF) relay operated spuriously. This spurious operation during energization was also confirmed on the other opposing bank when it was in service during this time.

Restricted earth fault protection is designed for fast and selective differential protection. Maximum availability of these capacitor banks for service requires reliable protection which will isolate the capacitor bank from the system before it is exposed to severe damage and certainly before a fault is established on the system. Spurious protection operations can hinder a plant’s availability and in some cases cause adverse system conditions on the network. Analyzing every unexplained relay operation (even when the cause seems apparent) builds a knowledge base and insight into the operation of the protective schemes that can pay off in the future [3].

II. RESEARCH STATEMENT

The investigation primarily focuses on Hydra Substation’s 400kV 100 MVAR Shunt Capacitor Bank in conjunction with the design of the REF protection circuit and high impedance REF protection relay operation. The SCB also uses a controlled switching technique for energizing the bank. The aim is to investigate spurious tripping events which occurred on the bank caused by REF protection operations, recommendations can then be made if any possible problems can be identified.

III. METHODOLOGY

A examination into the design of capacitor banks and capacitor protection philosophies was conducted in order to become acquainted with the technology and practices that are currently used. A collection of plant data was performed in order to collect all applicable data from site. This includes current transformer (CT) specification and REF relay characteristics etc. A comtrade energizing recording was made of the SCB. The applicable source impedance for the network was derived from the networks Digsilent model. This information was required to perform various analytical and mathematical calculations in order to verify inrush and setting calculations. An equivalent model was constructed in PSCAD and simulated and results used as a comparative measuring tool against the calculated and recorded energizing values. The REF relay response to the recorded waveforms was tested as well as its capability to filter out harmonics commonly found during capacitor bank energizing conditions.
IV. Power System Configuration

Fig 1. Single line diagram of the capacitor bank connected to 400kV busbar.

Power system parameters used in the simulation were sourced from the Eskom Transmission Digsilent model. Parameters seen below in Table I where derived by applying a three phase balanced fault on the busbars supplying the capacitor bank. A single phase fault was also applied to obtain the zero phase sequence impedance. This is done in order to derive an equivalent source impedance to be used when conducting the software simulations in PSCAD. Various switching scenarios where conducted to investigate the SCB energizing transient current behaviour.

Table I: Equivalent source and source impedance parameters derived from Digsilent for a symmetrical three phase fault on the busbars supplying the capacitor bank.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>Ipk</td>
<td>17296 A</td>
</tr>
<tr>
<td>Skss</td>
<td>11983.106 MVA</td>
</tr>
<tr>
<td>R</td>
<td>3.581 Ω</td>
</tr>
<tr>
<td>X</td>
<td>13.057 Ω</td>
</tr>
<tr>
<td>Z</td>
<td>15.539 Ω</td>
</tr>
<tr>
<td>Cos θ</td>
<td>0.74663</td>
</tr>
<tr>
<td>X/R ratio</td>
<td>19.48</td>
</tr>
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</table>

Equivalent source and source impedance parameters derived from Digsilent for a symmetrical three phase fault on the busbars of the network.

Layout of 100 MVar 400kV the capacitor bank is seen in fig 1 and typically contains the following elements seen below in Table II to Table V.

Table II: Capacitor Bank Technical Data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Single Can</th>
<th>Total Bank</th>
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</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>Westingcorp</td>
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<tr>
<td>Reactive Power</td>
<td>479kVAR</td>
<td>95.9MVAR</td>
</tr>
<tr>
<td>Nominal Voltage</td>
<td>17.321kV</td>
<td>400kV</td>
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<tr>
<td>Nominal capacitance</td>
<td>5.082uF</td>
<td>1.908uF</td>
</tr>
<tr>
<td>Nominal current</td>
<td>27.653A/unit</td>
<td>138.434A</td>
</tr>
</tbody>
</table>

Shunt capacitor bank arrangement:
Configuration: Single Star Earthed
Between phases: ungrounded single wye
Number of units in series: 16
Strings per phase: 6
Number of CAP. elements in parallel per can: 3
Number of CAP. elements in series per can: 9

Table III: Reactor Technical Data

<table>
<thead>
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<th>Parameter</th>
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<tr>
<td>Manufacturer</td>
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<td>Nominal Inductance</td>
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<td>Nominal Impedance</td>
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<td>Nominal Current</td>
<td>200A</td>
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TABLE IV: SURGE ARRESTER TECHNICAL DATA

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<td>Manufacturer</td>
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<td>Nominal Discharge Current</td>
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<tr>
<td>Energy Capability</td>
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TABLE V: SURGE CAPACITOR TECHNICAL DATA

<table>
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<tr>
<th>Parameter</th>
<th>Single Can</th>
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<td>Reactive Power</td>
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<tr>
<td>Nominal Voltage</td>
<td>825V</td>
<td>3.3kV</td>
</tr>
<tr>
<td>Nominal capacitance</td>
<td>781uF</td>
<td>3124uF</td>
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</table>

Technical data listed above is necessary for the creation of an equivalent model. In essence this is a basic RLC type circuit to which RLC transient theory can be applied. The capacitor bank also has current and voltage transformers (VT) installed for secondary signaling purposes. The only area of interest with these will be the current transformer cores used for the restricted earth fault protection.

V. Restricted Earth Fault Circuit

High impedance REF protection is used on the SCB which uses a circulating current operating principle. Its zone of protection lies between the current transformers which encompass the plant which it is protecting as seen below in fig 2.

In this case it includes the capacitor bank along with the current limiting reactor and earthing capacitors as well as the surge arrestors. The high impedance REF relay used in this application is a Siemens 7VH60 it is assumed that its burden is purely resistive as in the case of modern static or numerical protection. This was confirmed in the relay manual and is 1200Ω with a operating current of 20mA at a respective settable voltage. This operate current is irrespective of the voltage setting, but would exclude current drawn by the varistor installed in parallel with the element. A varistor is used to limit the voltage across the relay and CT terminals under abnormal conditions. In essence the basic operation of the relay is as follows. The secondary measured AC signal from the CT’s is connected through a low band pass filter then rectified to a DC voltage, this level is monitored by a Schmitt trigger and if it exceeds the set value will cause the relay to operate.

In theory the resultant current flowing into the relay from the current transformers under normal conditions is thought to be
zero. This is not always the case due to slight inaccuracies in the CT’s but the value of this spill current should be very low, only a few milliamps if the connections are correct. It is also desirable that the lead and winding resistance of the CT’s either side of the relay element be identical, this is not always achievable in practice. In this case the measured spill current was very small in order of 4mA. During a fault condition within the protected zone a reversal in current direction and magnitude is experienced. This causes a residual current to flow in the circuit into the relay. If the current is greater than the setting configured into the relay a trip command is issued for this specific application.

A. Current Transformer Requirements

A protection scheme’s reliable operation is also fundamentally dependent on the protection relays analog input sources which are provided by the current or voltage transformers. A requirement for older type REF protection is the matching of current transformer characteristics. This is normally performed to ensure limited spill current during heavy through fault conditions. For the circuit under instigation the current transformers differ. The neutral current transformer is of a different manufacturer and type.

B. Setting Calculations for REF relay

A selected voltage setting on the relay should exceed the voltage across the relay terminals for inrush current conditions. IEEE standard [4] introduces equations that are beneficial in the calculation of capacitor bank inrush currents. These calculations are important as they indicate what the magnitude of the maximum theoretical current in the circuit will be under energizing conditions. This is of particular importance as it can directly influence protection performance. Nominal current in the bank $I_{\text{rated}}$ is calculated as follows where $V_{L_L}$ is the rated system voltage and $Z_{\text{bank}}$ the impedance of the SCB:

$$I_{\text{rated}} = \frac{V_{L_L}}{\sqrt{3} \times Z_{\text{bank}}}$$  \hspace{1cm} (1)

Peak inrush current $I_{\text{max peak}}$ for the energizing of a single or parallel SCB without damping in Amperes is calculated below in eq (2). In practical circuits, it will be about 90% of this value.

$$I_{\text{max peak}} = 1000 \times V_{L_L} \times \sqrt{2} \times \sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}}$$  \hspace{1cm} (2)

For single bank energizing the maximum peak inrush current is limited by $L_{\text{eq}}$ the systems source inductance. However for back to back energizing the equivalent inductance $L_{\text{eq}}$ is now between the two locally connected SCB and is significantly smaller. $C_{\text{eq}}$ the equivalent capacitance also changes in the back to back energizing scenario and is the sum of the two banks in series. Smaller values of $L_{\text{eq}}$ and $C_{\text{eq}}$ gives rise to much larger inrush current. Using the above equations the following is calculated:

<table>
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<th>TABLE VI: INRUSH CURRENT MAGNITUDE’S AND FREQUENCY</th>
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<tr>
<td>$I_{\text{rated}}$</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>$I_{\text{max peak}}$</td>
</tr>
</tbody>
</table>

Single bank energising current transients of 5 – 20 p.u have been experienced. Furthermore if another SCB bank is energized in close proximity to a previously energized capacitor bank further considerations for inrush current need to be addressed. In the case of back to back energizing transient currents of 40 - 100 p.u have been experienced. The magnitude and frequency of this inrush current is, therefore, much higher than the inrush of an isolated capacitor bank [5]. This multiplication factor figure for inrush conditions is not found in the relay manual for SCB applications as its application is intended for classical REF applications. Inrush current during commissioning was modestly calculated using an assumed factor of 10 as follows:

$$I_{\text{inrush}} = 10 \times I_{\text{rated}}$$  \hspace{1cm} (3)

And the relay setting voltage formula obtained from the relay manual is Equal to:

$$V_{\text{eff}} > \frac{I_{\text{inrush}}}{CT\text{ratio}} \times (R_{\text{CT}} + 2 \times R_{\text{LEAD}})$$  \hspace{1cm} (4)

The particular ratios and kneepoints from the CT manufactures nameplates can be seen above in table VI. It must be mentioned that the test set used for testing and obtaining the magnetization curves is only rated up to 2 kV. Therefore it could not derive the kneepoint on the full ratio of 2400:1 for the phase post type current transformers.

### Table VI: REF Circuit CT Information

<table>
<thead>
<tr>
<th>Type</th>
<th>Neutral CT</th>
<th>Phase CT’s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer:</td>
<td>Britech S.A</td>
<td>Areva</td>
</tr>
<tr>
<td>kPV :</td>
<td>400 - 23mA</td>
<td>2.4kV - 42mA</td>
</tr>
<tr>
<td>Ratio :</td>
<td>1/400</td>
<td>1/400</td>
</tr>
<tr>
<td>Rs :</td>
<td>1.6</td>
<td>2.4</td>
</tr>
</tbody>
</table>

The magnetizing currents for the CT burdens are as follows:

- **Neutral Burden**: Rs = 0.01 A/0.1 V
- **R ph CT Burden**: Rs = 1.0 A/0.1 V
- **W ph CT Burden**: Rs = 1.0 A/0.1 V
- **B ph CT Burden**: Rs = 1.0 A/0.1 V

It can be seen from fig 3 that the current transformers magnetizing impedances differ from each other. Satisfactory operation is not attainable simply on matching the current transformers, as unbalance is also caused by the nonlinearity of the excitation characteristics.

![Impedance plot of secondary windings of current transformers](image-url)
Where $V_{eff}$ is the setting voltage, required to exceed voltage across relay during inrush. As seen from eq (3) the assumption of $I_{inrush}$ will directly affect the value of the required setting voltage and affects further calculations. Furthermore this selected factor does not cater for double bank energizing conditions. The effective primary current $I_{eff}$ at a particular setting equals the magnetizing current drawn by the four current transformers at the voltage setting. These currents are obtained from the magnetization curve using the voltage setting and the current drawn by the varistor at the calculated voltage setting. As shown below

$$I_{eff} = \left[ 3 \times \frac{I_{ct \ phases} + I_{ct\ neutral}}{2} + I_{relay} + I_{var} \right] \times CT\ ratio \quad (5)$$

Current drawn for the $V_{eff}$ value of voltage in the phase current transformers will be as follows:

$$I_{ct\ phases} = V_{eff} \times \left( \frac{I_{knee\ phases}}{V_{knee\ phases}} \right) \quad (6)$$

Current drawn for the $V_{eff}$ value of voltage in the neutral current transformers will be as follows:

$$I_{ct\ neutral} = V_{eff} \times \left( \frac{I_{knee\ neutral}}{V_{knee\ neutral}} \right) \quad (7)$$

Current drained by the varistor is calculated as follows

$$I_{var} = \left( \frac{V_{eff}}{K} \right)^B \quad (8)$$

Where B and K are constants attributed to the varistor of a certain type and K = 320 anb B = 0.25. This obtained from the relay manual [6]. Settings where calculated using the above formula.

### Table X: REF Setting Circuit Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ct\ phases}$</td>
<td>0.42 mA</td>
</tr>
<tr>
<td>$I_{ct\ neutral}$</td>
<td>1.38 mA</td>
</tr>
<tr>
<td>Kneepoint voltage Neutral CT</td>
<td>400V</td>
</tr>
<tr>
<td>Kneepoint voltage Phasel CT</td>
<td>2400V</td>
</tr>
<tr>
<td>Lead Resistance ($R_{lead}$)</td>
<td>5 (measured on site)</td>
</tr>
<tr>
<td>CT secondary Resistance ($R_{ct}$)</td>
<td>1.6 (measure on site)</td>
</tr>
<tr>
<td>Varistor Constant K</td>
<td>320</td>
</tr>
<tr>
<td>$I_{var}$</td>
<td>0.000031640625</td>
</tr>
<tr>
<td>$I_{neutral}$</td>
<td>1384.34</td>
</tr>
<tr>
<td>$V_{eff}$</td>
<td>22.8 V available setting 24V</td>
</tr>
</tbody>
</table>

A recommendation for the relay manual is that the kneepoint voltage of the current transformer must be at least twice relay setting voltage to ensure reliable operation. In this case it equates to 48V which is substantially lower than the kneepoint [6].

VII. CONTROLLED SWITCHING

The SCB makes use of controlled switching. This technique uses an electronic control device to control closing of the circuit breaker. Time displacement between phases for a balanced three phase system of these zero crossing points transpires every 60°. For a 50Hz signal this is approximately 3.33 milliseconds. [7] It must also however be noted that the closing speed of the breaker is dependent on its mechanical characteristics. Small delays between close commands and breaker switch closing are commonly experienced. Breaker closing speeds can range from 16-100ms. It is desirable that a circuit breakers operation be fairly consistent and repeatable in controlled switching applications. The regularity should fall within two milliseconds. [5]

The requirements which must be fulfilled by the controlled switching arrangement for the limitation of the maximum transients below acceptable limits in a grounded neutral capacitor back-to-back energization case are the following:

- Maximum deviation of starting instant of contacts movement ($\Delta T$) ±1 ms in conjunction with a relatively “fast” switching device with a Rate-of-Decay of Dielectric Strength (RDDS) greater than 1.1 per unit or Maximum $\Delta T$ of ±0.5 ms in conjunction with a more “slow” (and thus common) switching device with a RDDS greater than 0.75 per unit. It can be mentioned succinctly, that the main requirement for effective application of synchronized switching is the use of controlled switching arrangements with quite small deviation of starting instant of contacts movement and high contact speed. With this requirement fulfilled, a very sufficient reduction of the dc current components and high frequency inrush currents and transient overvoltage’s appearing after the energization of reactors and capacitors, respectively, is achieved, but only for grounded neutral cases. [8]

VIII. REF AND SYNCHRONIZED SWITCHING

Due to the sensitive nature of REF circuits in circulating current configurations stability during energizing may prove to be troublesome. It must however be noted that in this application the REF circuit is subjected to a brief imbalance in currents during the energizing of the SCB. The recording below in Fig 4 shows the brief imbalance which occurs in the REF circuit during the closing sequence. This is the resultant voltage which appears across the relay terminals.

![Image](image-url)

*Fig. 4 Voltage appearing across varistor connected in parallel to REF relay element. The three distinctive peaks correlate to the closing sequence of the three breaker poles.*

For a balanced three phase system the resultant sum of all three phases is said to be zero. Therefore during the closing transition of the each pole the transitory resultant values are not zero due to staggered switching. The following equation represents the magnitude of current that would be experienced on a per phase basis.

$$i = \sqrt{2} \times I_{pdc} \left[ e^{-\frac{t}{\tau}} \cos(\phi - \alpha) - (\cos \omega t + \phi - \alpha) \right] \quad (9)$$
Where $\varphi = \text{Angle of switching on the voltage curve}$ $I_{psc} = Vm/(R^2 + \omega^2 L^2)^{1/2}$ the r.m.s. value of primary symmetrical short circuit current $T_p = L/R$ is the primary time constant and $\alpha = \tan^{-1}(\omega L/R)$ is the phase angle difference between voltage and current. It can be seen that the angle of $\varphi$ will directly effect the magnitude of $I_{psc}$. The first part of the term is the transient component of the waveform and the second part is the steady state. The transient component will be zero when $(\varphi - \alpha) = \pm \pi/2$ and will have a maximum when $(\varphi - \alpha) = 0$. Assuming the network predominantly inductive it is preferable for switching to take place on voltage wave when passing through maximum and zero. [9]

IX. SOFTWARE MODEL

A single bank simplified capacitor bank model below in fig 5 was created in PSCAD ver 4.2. Controlled switching was implemented by staggering the circuit breaker closing times via delay blocks. This was done to try and replicate the point of wave synchronizing relay implemented on site. Delays where set to the recorded switching times from site. Two scenarios where simulated, being single and double bank energizing at the local substation.

![Fig. 5. The model built in PSCAD](image)

X. CASE STUDY PSCAD AND SITE RECORDINGS

Because there is no fault recording capabilities on the current protection scheme, a digital fault recording was taken during the energizing of the SCB. This included the respective voltages and currents for the bay. Recordings where taken at a sufficient 9kHz sampling frequency. Current recordings where taken using external type clip on current transformers the Omicron C-Probe 1 current clamp. These too have certain accuracy levels and this is considered. Clip on type CT’s are preferable as they are noninvasive and do not disturb the commissioned CT circuits. Voltage measurements in Fig 5 were taken from secondary busbar VT circuits. Recording of a comtrade file was done via a Omicron 356 used in conjunction with Omicron Enerlizer software. The test trigger condition was a current threshold level. When the threshold is exceeded the recording is started and buffered waveform is captured.

![Fig. 5. Secondary voltages recorded on the 400kV busbar at site during single bank energization. The bank is switched in at t = 0ms](image)

![Fig. 6. Simulated recorded secondary voltages for energization in PSCAD simulation.](image)

XI. REF RELAY TEST

A 7VH60 relay uses a low pass filter on its analog input. Testing of the relay included injecting analog signals rich in harmonics and checking the relays response. It was found that the relay operated at a substantially lower voltage of 7.5V at 50Hz with harmonic content of 20% up to the 60th harmonic. It did however prove to be quite accurate when injecting the setting voltage of 24V at a fundamental frequency of 50Hz. Relay operate times of between 25ms and 40ms where experienced for injected faults. Poor filter design was later confirmed by the manufacturer, who advised that the relay had been discontinued due to poor performance regarding its filtering circuitry. For protective relays which rely on precise fundamental quantity’s post fault voltages and currents need to be extracted as quickly and as accurately as possible. An ideal filter is a narrow band pass filter [10].

XII. ANALYSIS OF RECORDED AND SIMULATED RESULTS

Recordings of the phase currents taken during energization of the single SCB are seen below in Fig 7

![Fig. 7. Secondary recorded current waveforms for phase currents measured on site during single bank energizing. The high frequency oscillation and peaks during switching can be clearly seen.](image)
After a period of approximately one and a half cycles or 30ms the circuit stabilizes. This is dependent on the damping ratio of the network and will change as the network changes or is configured. These currents create a voltage across the REF relay during the breaker closing sequence. The presence of this voltage across REF relay disappears once all three breakers poles are successfully closed. This voltage is however lower than the setting voltage of 24V. Which is correct as the relay did not trip in this case. However in the case as back to back energizing conditions a much larger magnitude of transient current is present. This is seen in the simulated waveform below in Fig 8.

![Simulated switching transient for energizing of a single bank](image)

Fig 8 Simulated switching transient for energizing of a single bank. After a few milliseconds another bank is energized at the local substation approximately 100ms later. Magnitudes of the second set of currents are seen through both SCB line current transformers.

A 1ms delay in closing of a breaker pole on the voltage waveform is enough to produce a substantial transient current. This is even worse in the case of back to back energizing. This in turn will create a spill current in the REF relay circuit. If closing is delayed long enough the effective transient current may be enough to cause relay operation.

XIII. CONCLUSIONS

REF protection is not classically applied to SCB’s so its characteristics and requirements should be carefully considered. When energizing a single isolated capacitor bank from predominantly inductive source. It can be noted that a high-frequency, high-magnitude current flows into the capacitor bank this can attributed to the fact that the bank is trying to equalize the system voltage and the capacitor voltage [7]. These inrush currents may cause CT saturation if they are of a substantially large magnitude. Careful consideration should also be made when selecting protection relays. As inadequate filtering of harmonics will affect the protection circuits performance. Older type static relays using exclusively low pass filters may prove to be troublesome as their performance may diminish with high harmonic currents. Controlled switching may pose a potential problem for protection circuits especially in REF if closing time delays are exceeded and switching takes place on higher points of the voltage wave. As seen in the setting calculations the inrush current in eq (3) will play a pivotal role in the selection of the voltage setting. It may be reasonable to sacrifice sensitivity in terms protection settings for increased security. This however is dependent on the nature of the plant being protected. In this case the setting needs to be increased to a sufficient value for double bank energizing conditions calculated to be 96V. A block signal can also be added for the duration of the beaker close sequence. This would need to be linked to both banks for double bank energizing conditions and block a REF trip during the point on wave switching. A modern solution would be to replace the relay with a modern numerical high impedance REF relay. These have digital filters and can filter out the large amounts of high frequency inrush currents associated with SCB energizing. They also have built in fault recording capabilities which aid greatly in post fault investigation.

XIV. REFERENCES


XIII. BIOGRAPHIES

Warick Minkley has a Bachelor Technologae Degree from UNISA University of South Africa. He has been with Eskom Distribution since 2005. He is a registered Professional Technician with Engineering Council of South Africa. He’s interests include power system protection.